DYNAMIC MEMORY CONTROLLER 2964B

FEATURES

- **Operating Flexibility—controls 16K or 64K dynamic RAMSs**
- **8-Bit Refresh Counter—refresh address generation, clear input, and selectable terminal count (128 or 256) output**
- **Row Address Decoder—four active Row Address Select (RAS) outputs during refresh**
- **On-Chip Latches—dual 8-bit address latches and RAS decoder latches**
- **User-Selectable Refresh Modes—burst, distributed, or transparent**
- **3-port, 8-bit address multiplexer with Schottky speed**
- **Non-inverting address for RAS and CAS signal paths**

PRODUCT DESCRIPTION

The Signetics 2964 Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation, and Row/Column control for MOS dynamic memories of any data width. The eight bit address path is designed for 64K RAMs but can be used equally well with 16K RAMs. Sixteen address input latches and two row address select latches (for higher order address) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal row address decoder to select from one-of-four banks of RAMs.

FUNCTIONAL OPERATION

The Signetics 2964B Dynamic Memory Controller (Figure 1) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the DRAM address lines.

The 2964B also includes a special RAS decoder and CAS buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The RAS Decoder allows upper addresses to select one-of-four banks of DRAM by determining which bank receives a RAS input. During refresh ($\overline{RFSH}$ = LOW), the decoder mode is changed to four-of-four and all banks of memory receive a RAS input for refresh in response to a RASI active LOW input. CAS is inhibited during refresh.

Burst mode refresh is accomplished by holding RFSH low and toggling RASI.

A_{15} is a dual function input which controls the refresh counter's range. For 64K DRAMs, it is an address input. For 16K DRAMs, it can be pulled to + 12V through 1K to terminate the refresh count at 128 instead of 256.

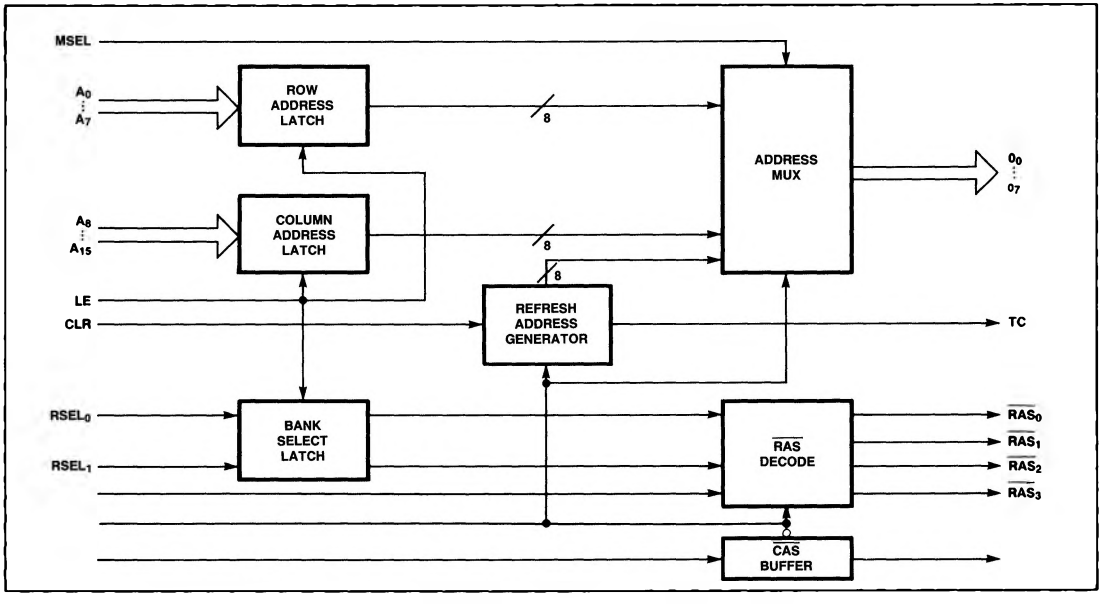

Figure 1. Block Diagram of 2964B Dynamic Memory Controller