

68HC705JB2

SPECIFICATION (General Release)

August 28, 1998

Consumer Systems Group
Semiconductor Products Sector

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1.2 MASK OPTIONS

The mask options on the MC68HC705JB2 are handled with five EPROM bits in the Mask Option Register (\$01FF). These options are:

- External interrupt pins ($\overline{\text{IRQ}}$, PA0 to PA3):
[edge-triggered or edge-and-level-triggered]
- Port A and port B pull-down/pull-up resistors:
[connected or disconnected]
- PA0-PA3 external interrupt capability:
[enabled or disabled]
- OSC, crystal/ceramic resonator startup delay:
[4064 or 128 internal bus cycles]
- Low Voltage Reset (LVR):
[enabled or disabled]

To program the MOR, the MORON bit in the Program Control Register (bit 3 of \$3E) must be set to "1".

	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0	
MOR \$01FF	Read				IRQTRIG	PULLREN	PAINTEN	OSCDLY	LVREN
	Write								
	Erased	0	0	0	1	1	1	1	1
	Reset	Unaffected							

IRQTRIG – IRQ, PA0-PA3 Interrupt Options

- 1 = Edge-trigger only
- 0 = Edge-and-level-triggered

PULLREN – Port A and B Pullup/Pulldown Options

- 1 = Connected
- 0 = Disconnected

PAINTEN – PA0-PA3 External Interrupt Options

- 1 = Disabled
- 0 = Enabled

OSCDLY – Oscillator Delay Option

- 1 = 128 internal clock cycles
- 0 = 4064 internal clock cycles

LVREN – LVR Option

- 1 = Enabled
- 0 = Disabled

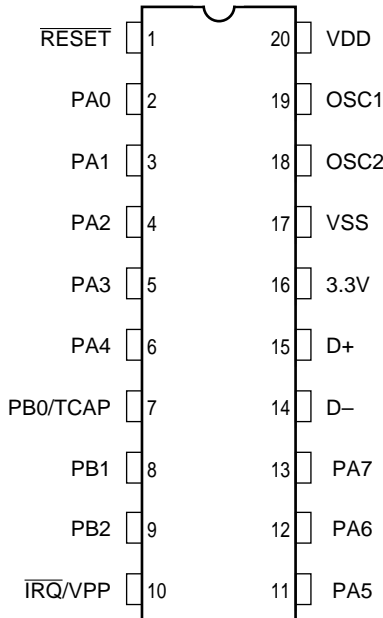


Figure 1-2. Pin Assignments for 20-Pin Package

1.4 FUNCTIONAL PIN DESCRIPTIONS

The following paragraphs give a description of the general function of each pin assigned in **Figure 1-2**.

1.4.1 V_{DD}, V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the positive supply, and V_{SS} is ground. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care should be taken to provide good power supply bypassing at the MCU by using bypass capacitors with good high-frequency characteristics that are positioned as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

1.4.2 OSC1, OSC2

The OSC1 and OSC2 pins are the connections for the on-chip oscillator. The OSC1 and OSC2 pins can accept the following sets of components:

components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion. An internal start-up resistor of 2M Ω (typical) is provided between OSC1 and OSC2 for the ceramic resonator type oscillator.

1.4.2.3 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-3(b)**.

1.4.3 $\overline{\text{RESET}}$

This is an I/O pin. This pin can be used as an input to reset the MCU to a known start-up state by pulling it to the low state. The $\overline{\text{RESET}}$ pin contains a steering diode to discharge any voltage on the pin to V_{DD} , when the power is removed. An internal pull-up is also connected between this pin and V_{DD} . The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. This pin is an output pin if LVR triggers an internal reset.

1.4.4 $\overline{\text{IRQ/VPP}}$

This input pin drives the asynchronous IRQ interrupt function of the CPU. The IRQ interrupt function has a mask option to provide either only negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering. If the option is selected to include level-sensitive triggering, the $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wired-OR" operation, if desired. The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

NOTE

Each of the PA0 thru PA3 I/O pins may be connected as an OR function with the IRQ interrupt function by a mask option. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{\text{IRQ}}$ pin, except for the inverted phase. The edge or level sensitivity selected by a separate mask option for the $\overline{\text{IRQ}}$ pin also applies to the I/O pins OR'ed to create the IRQ signal.

In Bootloader mode, this pin (VPP) is used to supply the required programming voltage to the EPROM array.

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GENERAL DESCRIPTION

MC68HC705JB2
REV 1.1

1-8

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2.2 I/O AND CONTROL REGISTERS

The I/O and Control Registers reside at locations \$0000-\$003F. The outline of these registers are shown in **Figure 2-2**. The bit assignments for each register are shown in **Figure 2-3**, **Figure 2-4**, and **Figure 2-5**. Reading from unimplemented bits will return unknown states, and writing to unimplemented bits will be ignored.

Port A Data Register	\$0000
Port B Data Register	\$0001
unimplemented (2)	
Port A Data Direction Register	\$0004
Port B Data Direction Register	\$0005
unimplemented (2)	
Timer Control & Status Register	\$0008
Timer Counter Register	\$0009
IRQ Control & Status Register	\$000A
unimplemented (5)	
Port A Pulldown Register	\$0010
Port B Pulldown/up Register	\$0011
Timer1 Registers (10)	\$0012 to \$001B
unimplemented (4)	
USB Endpoint0 Data Registers (8)	\$0020 to \$0027
USB Endpoint1 Data Registers (8)	\$0028 to \$002F
USB Control2 Register	\$0037
USB Address Register	\$0038
USB Interrupt0 Register	\$0039
USB Interrupt1 Register	\$003A
USB Control0 Register	\$003B
USB Control1 Register	\$003C
USB Status Register	\$003D
EPROM Program Control Register	\$003E
Reserved	\$003F
Mask Option Register	\$01FF

Figure 2-2. I/O Registers

Table 12-7. Opcode Map

MSB LSB	Bit Manipulation			Branch			Read-Modify-Write			Control			Register/Memory					
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	MSB LSB	
0	BRSTO DIR 2	BSETO DIR 2	BRA REL 2	NEG DIR 2	NEGA INH 1	NEGX INH 2	NEG IX1 1	NEG IX 1	RTI INH 9		SUB IMM 2	SUB DIR 3	SUB EXT 4	SUB IX2 5	SUB IX1 4	SUB IX 3	0	
1	BRCLRO DIR 2	BCLRO DIR 2	BRN REL 3						RTS INH 6		CMP IMM 2	CMP DIR 3	CMP EXT 4	CMP IX2 5	CMP IX1 4	CMP IX 3	1	
2	BRSET1 DIR 2	BSET1 DIR 2	BHI REL 3		MUL INH 11						SBC IMM 2	SBC DIR 3	SBC EXT 4	SBC IX2 5	SBC IX1 4	SBC IX 3	2	
3	BRCLR1 DIR 2	BCLR1 DIR 2	BLS REL 3	COM DIR 1	COMA INH 3	COMX INH 3	COM IX1 6	COM IX 5	SWI INH 10		CPX IMM 2	CPX DIR 3	CPX EXT 4	CPX IX2 5	CPX IX1 4	CPX IX 3	3	
4	BRSET2 DIR 2	BSET2 DIR 2	BCC REL 3	LSR DIR 1	LSRA INH 1	LSRX INH 1	LSR IX1 1	LSR IX 1			AND IMM 2	AND DIR 3	AND EXT 4	AND IX2 5	AND IX1 4	AND IX 3	4	
5	BRCLR2 DIR 2	BCLR2 DIR 2	BCS/BLO REL 3								BIT IMM 2	BIT DIR 3	BIT EXT 4	BIT IX2 5	BIT IX1 4	BIT IX 3	5	
6	BRSET3 DIR 2	BSET3 DIR 2	BNE REL 3	ROR DIR 1	RORA INH 1	RORX INH 1	ROR IX1 1	ROR IX 1			LDA IMM 2	LDA DIR 3	LDA EXT 4	LDA IX2 5	LDA IX1 4	LDA IX 3	6	
7	BRCLR3 DIR 2	BCLR3 DIR 2	BEQ REL 3	ASR DIR 1	ASRA INH 1	ASRX INH 1	ASR IX1 1	ASR IX 1	TAX INH 2		STA IMM 2	STA DIR 3	STA EXT 4	STA IX2 5	STA IX1 4	STA IX 3	7	
8	BRSET4 DIR 2	BSET4 DIR 2	BHCC REL 3	ASL/SL DIR 1	ASLA/SLA INH 1	ASLX/SLX INH 1	ASL/SL IX1 1	ASL/SL IX 1			EOR IMM 2	EOR DIR 3	EOR EXT 4	EOR IX2 5	EOR IX1 4	EOR IX 3	8	
9	BRCLR4 DIR 2	BCLR4 DIR 2	BHCS REL 3	ROL DIR 1	ROLA INH 1	ROLX INH 1	ROL IX1 1	ROL IX 1			ADC IMM 2	ADC DIR 3	ADC EXT 4	ADC IX2 5	ADC IX1 4	ADC IX 3	9	
A	BRSET5 DIR 2	BSET5 DIR 2	BPL REL 3	DEC DIR 1	DECA INH 1	DECX INH 1	DEC IX1 1	DEC IX 1			ORA IMM 2	ORA DIR 3	ORA EXT 4	ORA IX2 5	ORA IX1 4	ORA IX 3	A	
B	BRCLR5 DIR 2	BCLR5 DIR 2	BMI REL 3								ADD IMM 2	ADD DIR 3	ADD EXT 4	ADD IX2 5	ADD IX1 4	ADD IX 3	B	
C	BRSET6 DIR 2	BSET6 DIR 2	BMC REL 3	INC DIR 1	INCA INH 1	INCX INH 1	INC IX1 1	INC IX 1			RSP INH 2	JMP DIR 3	JMP EXT 3	JMP IX2 4	JMP IX1 3	JMP IX 2	C	
D	BRCLR6 DIR 2	BCLR6 DIR 2	BMS REL 3	TST DIR 1	TSTA INH 1	TSTX INH 1	TST IX1 1	TST IX 1			NOP INH 2	JSR DIR 3	JSR EXT 3	JSR IX2 7	JSR IX1 6	JSR IX 5	D	
E	BRSET7 DIR 2	BSET7 DIR 2	BIL REL 3						STOP INH 2		LDX IMM 2	LDX DIR 3	LDX EXT 3	LDX IX2 5	LDX IX1 4	LDX IX 3	E	
F	BRCLR7 DIR 2	BCLR7 DIR 2	BIH REL 3	CLR DIR 1	CLRA INH 1	CLR INH 1	CLR IX1 1	CLR IX 1				STX DIR 4	STX EXT 3	STX IX2 6	STX IX1 5	STX IX 4	F	

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

MSB of Opcode in Hexadecimal

MSB	0
LSB	BRSTO DIR 5

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

