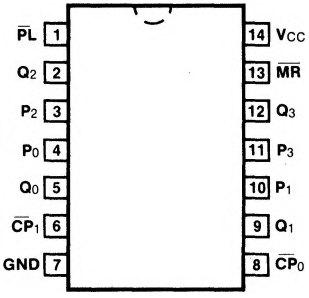
54/74176

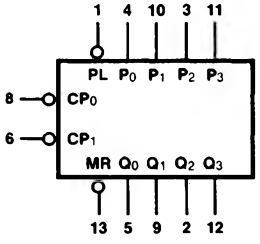
PRESETTABLE DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '176 is a presettable decade ripple counter partitioned into divide-by-two and divide-by-five sections, with separate clock inputs for the two sections. It can be connected to operate either in a BCD (8421) sequence or in a bi-quinary sequence producing a 50% duty cycle output. A LOW signal on the Master Reset ($\overline{MR}$) input overrides all other inputs and forces the Q outputs LOW. A LOW signal on the Parallel Load ($\overline{PL}$) input causes the Q outputs to assume the state of their respective Parallel Data (P_n) inputs, regardless of the clock. In the counting mode, state changes are initiated by the falling edge of the clock.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74176PC		9A
Ceramic DIP (D)	A	74176DC	54176DM	6A
Flatpak (F)	A	74176FC	54176FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs*	20/10

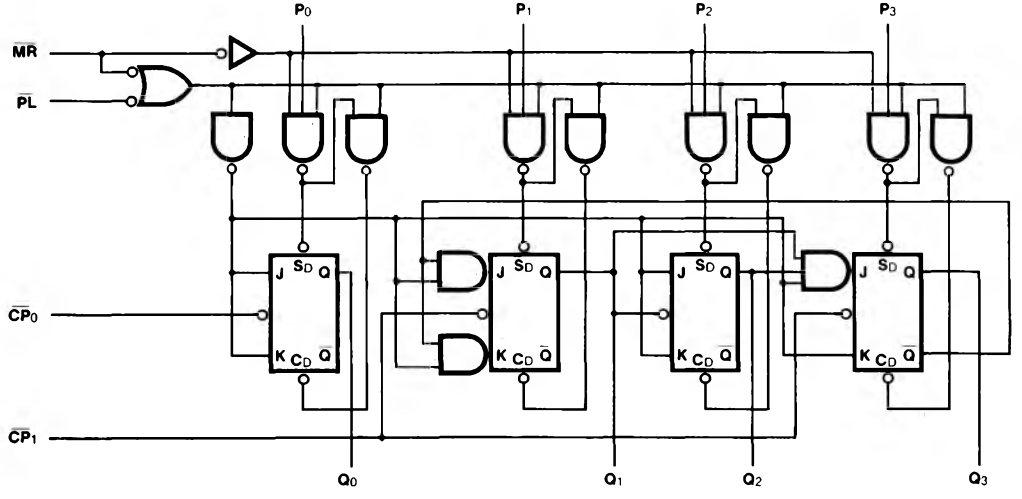
*Q_0 is guaranteed to drive $\overline{CP_1}$ in addition to the full rated load.

FUNCTIONAL DESCRIPTION — The '176 is an asynchronously presettable decade ripple counter partitioned into divide-by-two and divide-by-five sections. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop while the $\overline{CP}_1$ input serves the divide-by-five section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input.

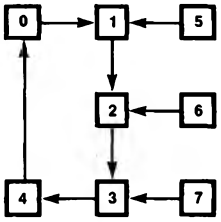
The '176 can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The '176 has an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P_0 — P_3) inputs into flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

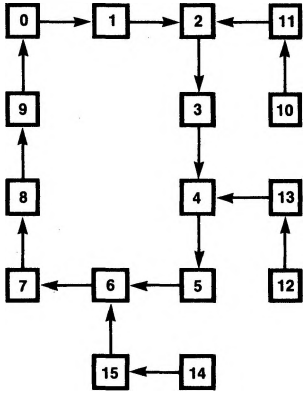
LOGIC DIAGRAM



÷5 STATE DIAGRAM



BCD STATE DIAGRAM



MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⊓	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
Icc	Power Supply Current		48	mA	Vcc = Max All inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency at $\overline{CP_0}$	35		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency at $\overline{CP_1}$	17.5		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0		13 17	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1		17 26	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2		41 51	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3 for '176		20 26	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3 for '177		66 75	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		29 46	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		43 48	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		48	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH P_n to $\overline{PL}$	15		ns	Fig. 3-13
t_h (H)	Hold Time HIGH P_n to $\overline{PL}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW P_n to $\overline{PL}$	20		ns	Fig. 3-13
t_h (L)	Hold Time LOW P_n to $\overline{PL}$	0		ns	Fig. 3-13
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	14		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	28		ns	Fig. 3-9
t_w (L)	$\overline{PL}$ Pulse Width LOW	25		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ or $\overline{PL}$ to $\overline{CP_n}$	25		ns	Fig. 3-16