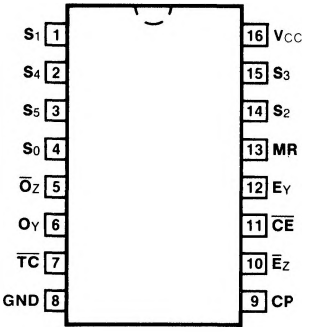
54/7497

SYNCHRONOUS MODULO-64 BIT RATE MULTIPLIER

DESCRIPTION — The '97 contains a synchronous 6-stage binary counter and six decoding gates that serve to gate the clock through to the output at a sub-multiple of the input frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S_0 — S_5) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. An asynchronous Master Reset input prevents counting and resets the counter.

CONNECTION DIAGRAM
PINOUT A



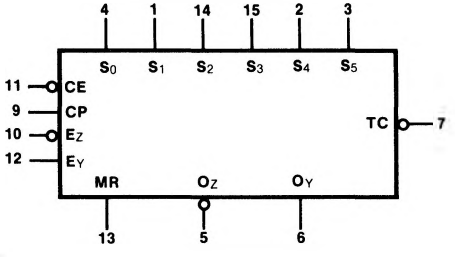
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7497PC		9B
Ceramic DIP (D)	A	7497DC	5497DM	7B
Flatpak (F)	A	7497FC	5497FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0 — S_5	Rate Select Inputs	1.0/1.0
$\overline{E}_Z$	$\overline{O}_Z$ Enable Input (Active LOW)	1.0/1.0
E_Y	O_Y Enable Input	1.0/1.0
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0
$\overline{O}_Z$	Gated Clock Output (Active LOW)	10/10
O_y	Complement Output (Active HIGH)	10/10
$\overline{TC}$	Terminal Count Output (Active LOW)	10/10

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

FUNCTIONAL DESCRIPTION — The '97 contains six JK flip-flops connected as a synchronous modulo-64 binary counter. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (63), with all Qs HIGH, the Terminal Count ($\overline{TC}$) output will be LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset (MR) resets the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S_5 is HIGH.

The flip-flop outputs are decoded by a 6-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select ($S_0 - S_5$) inputs. The Z output, $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled by the counter at different times and different rates relative to the clock. For example, the gate to which S_5 is connected is enabled during every other clock period, assuming S_5 is HIGH. Thus, during one complete cycle of the counter (64 clocks) the S_5 gate is enabled 32 times and can therefore gate 32 clocks per cycle to the output. The S_4 gate is enabled 16 times per cycle, the S_3 gate 8 times per cycle, etc. The output pulse rate thus depends on the clock rate and which of the $S_0 - S_5$ inputs is HIGH.

$$f_{out} = \frac{m}{64} \bullet f_{in}$$

$$\text{Where: } m = S_5 \bullet 2^5 + S_4 \bullet 2^4 + S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0$$

Thus by appropriate choice of signals applied to the $S_0 - S_5$ inputs, the output pulse rate can range from 1/64 to 63/64 of the clock rate, as suggested in the Rate Select Table. There is no output pulse when the counter is in the "all ones" condition. When m is 1, 2, 4, 8, 16 or 32, the output pulses are evenly spaced, assuming that the clock frequency is constant. For any other value of m the output pulses are not evenly spaced, since the pulse train is formed by interleaving pulses passed by two or more of the AND gates. The Pulse Pattern Table indicates the output pattern for several values of m. In each row, a one means that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero means that $\overline{O}_Z$ will be LOW when the clock is LOW in that period. The first column in the output field coincides with the "all zeroes" condition of the counter, while the last column represents the "all ones" condition. The pulse pattern for any particular value of m can be deduced by factoring it into the sum of appropriate powers of two (e.g. 19 = 16 + 2 + 1) and combining the pulses (i.e., the zeroes) shown for each for the relevant powers of two (e.g., for m = 16, 2 and 1).

The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input, E_Y, disables O_Y. To expand the multiplier to 12-bit rate select, two packages can be cascaded as shown in *Figure a*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only 1/64 the rate of the first and a full cycle of the two counters combined requires 4096 clocks. Each rate select input of the first package has 64 times the weight of its counterpart in the second package.

$$f_{out} = \frac{m_1 + m_2}{64 \bullet 64} \bullet f_{in}$$

$$\text{Where: } m_1 = S_5 \bullet 2^{11} + S_4 \bullet 2^{10} + S_3 \bullet 2^9 + S_2 \bullet 2^8 + S_1 \bullet 2^7 + S_0 \bullet 2^6 \text{ (first package)}$$

$$m_2 = S_5 \bullet 2^5 + S_4 \bullet 2^4 + S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0 \text{ (second package)}$$

Combined output pulses are obtained in *Figure a* by letting the Z output of the first circuit act as the Y-enable function for the second, with the interleaved pulses obtained from the Y output of the second package being opposite in phase to the clock.

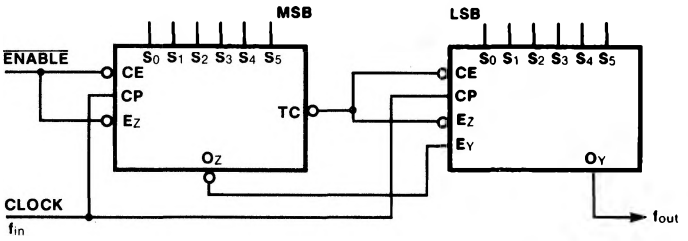
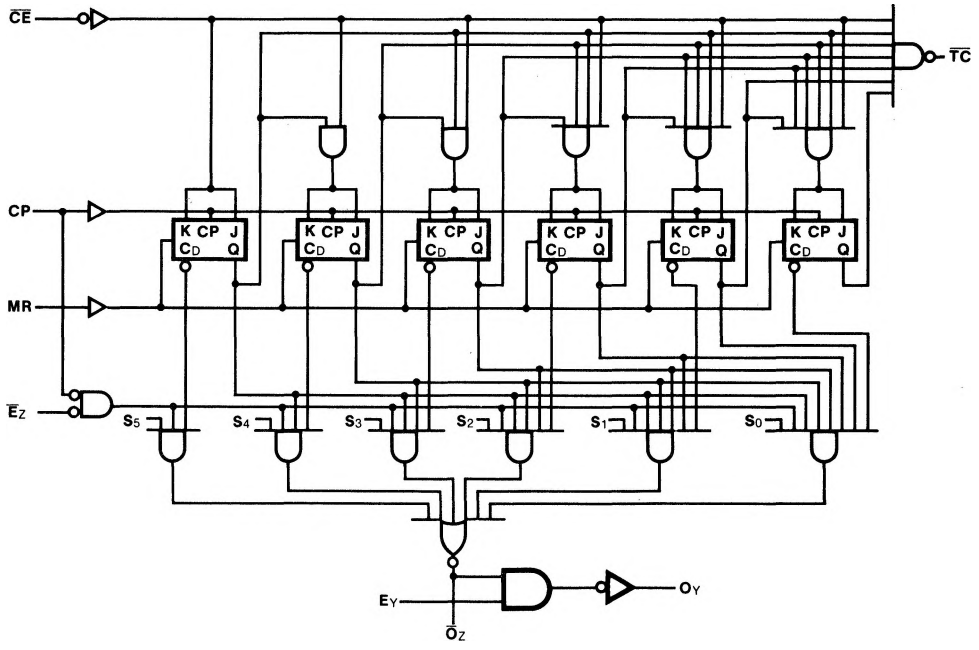


Fig. a. Cascading for 12-bit Rate Select

LOGIC DIAGRAM



MODE AND RATE SELECT TABLE (Note 1)

INPUTS									CLOCK PULSES	OUTPUTS				NOTES
MR	$\overline{CE}$	$\overline{E_Z}$	S_5	S_4	S_3	S_2	S_1	S_0		E_Y	O_Y	$\overline{O_Z}$	$\overline{TC}$	
H	X	H	X	X	X	X	X	X	X	H	L	H	H	2
L	L	L	L	L	L	L	L	L	64	H	L	H	1	3
L	L	L	L	L	L	L	L	H	64	H	1	1	1	3
L	L	L	L	L	L	L	H	L	64	H	2	2	1	3
L	L	L	L	L	L	H	L	L	64	H	4	4	1	3
L	L	L	L	L	H	L	L	L	64	H	8	8	1	3
L	L	L	L	H	L	L	L	L	64	H	16	16	1	3
L	L	L	H	L	L	L	L	L	64	H	32	32	1	3
L	L	L	H	H	H	H	H	H	64	H	63	63	1	3
L	L	L	H	H	H	H	H	H	64	L	H	63	1	4
L	L	L	H	L	H	L	L	L	64	H	40	40	1	5

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:
1. Numerals indicate number of pulses per cycle.
2. This is a simplified illustration of the clear function. CP and $\overline{E_Z}$ also affect the logic level of O_Y and $\overline{O_Z}$. A LOW signal on E_Y will cause O_Y to remain HIGH.
3. Each rate illustrated assumes S_0 — S_5 are constant throughout the cycle; however, these illustrations in no way prohibit variable-rate operation.
4. E_Y is used to inhibit output Y.
5. $f_{out} = m \bullet \frac{f_{in}}{64} = \frac{(32 + 8)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

PULSE PATTERN TABLE

m	OUTPUT PULSE PATTERN AT $\overline{O_Z}$
1	11111111111111111111111111111101111111111111111111111111111111
2	11111111111111101111111111111111111111111111111101111111111111
3	11111111111111101111111111111101111111111111111011111111111111
4	11111110111111111111111011111111111111101111111111111110111111
5	11111110111111111111111011111110111111101111111111111110111111
6	11111110111111101111111011111111111111101111111011111111011111
8	11101111111011111110111111101111111011111110111111101111110111
10	11101111111011101110111111101111111011111110111011101111110111
12	11101110111011111110111011101111111011101110111111101110111011
14	11101110111011101110111011101111111011101110111011101110111011
16	10111011101110111011101110111011101110111011101110111011101011
20	10111010101110111011101010111011101110101011101110111011101011
24	10101011101010111010101110101011101010111010101110101011101011
28	10101010101010111010101010101011101010101010101110101010101011
32	010101.... 0101

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-18	-55	mA	V_{CC} = Max
I_{CC}	Power Supply Current		120	mA	V_{CC} = Max All Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to $\overline{O}_Z$		18 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to O_Y		30 33	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E_Y to O_Y		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to O_Y		23 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{O}_Z$		14 14	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay CP to O_Y		39 30	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_Z$		18 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 33	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{TC}$		20 21	ns	Figs. 3-1, 3-5
t_{PLH}	Propagation Delay MR to O_Y		36	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay MR to $\overline{O}_Z$		23	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Rising	25		ns	Fig. b
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Rising	0	t_w CP -10	ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Falling	0	t_w CP -10	ns	Fig. c
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Falling	20	T -10	ns	
t_{inh} (H)	Inhibit Time HIGH $\overline{CE}$ to CP Falling	10		ns	Fig. b
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (H)	MR Pulse Width HIGH	15		ns	Fig. 3-16

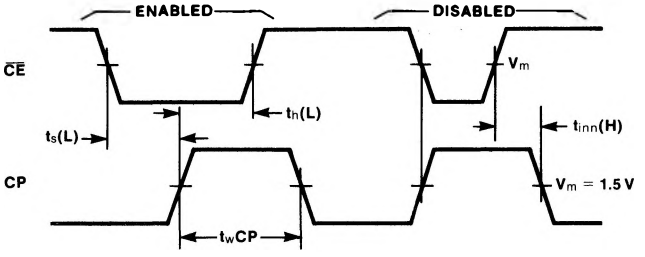


Fig. b

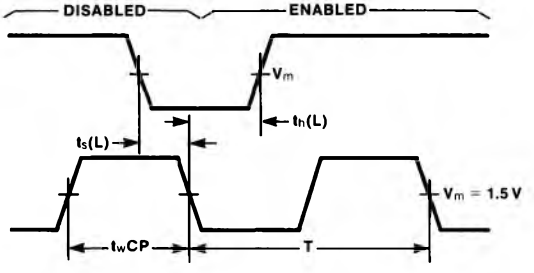


Fig. c