National Semiconductor

ADVANCE INFORMATION

54AC/74AC2525 • 54AC/74AC2526
Minimum Skew Clock Driver

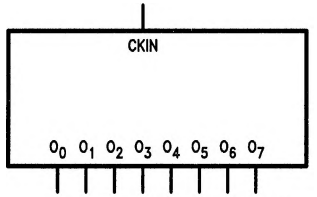
The 'AC2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The 2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the TPLH and TPHL transitions. The AC2526 is similar to the AC2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

Features

- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- 24 mA output drive capability

Logic Symbols

'AC2525



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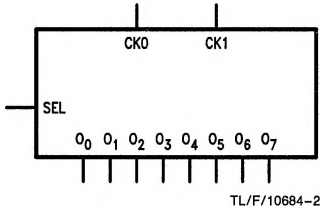
'AC2526



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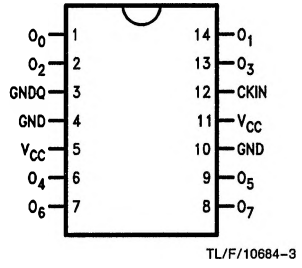
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

'AC2525



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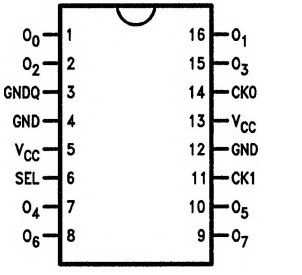
'AC2526



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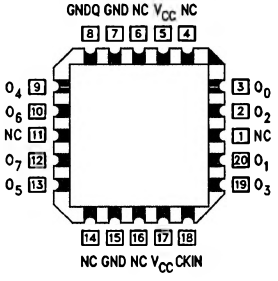
Pin Assignment for LCC



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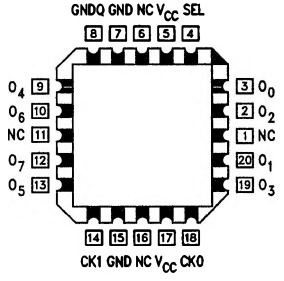

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