

# 74ACT11867

## SYNCHRONOUS 8-BIT UP/DOWN BINARY COUNTER WITH ASYNCHRONOUS CLEAR

SCAS178A – DECEMBER 1991 – REVISED FEBRUARY 1998

- Inputs Are TTL-Voltage Compatible
- Asynchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

### description

The 74ACT11867 is a synchronous presettable binary counter featuring an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

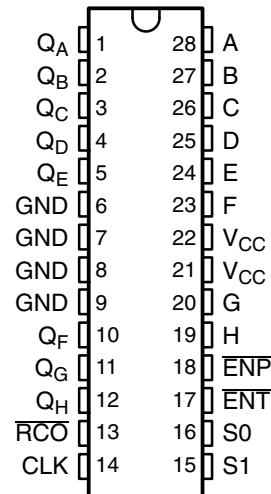
The counters are fully programmable; that is, the outputs can each be preset to either logic level. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock rising edge.

The carry look-ahead circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. This is done with two count-enable inputs and a carry output. Both count-enable ( $\overline{ENP}$  and  $\overline{ENT}$ ) inputs must be low to count. The direction of the count is determined by the levels of the select (S0 and S1) inputs (see the function table). Input  $\overline{ENT}$  is fed forward to enable the ripple-carry ( $\overline{RCO}$ ) output.  $\overline{RCO}$  then produces a low-level pulse while the count is zero (all outputs low) when counting down or 255 during counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at  $\overline{ENP}$  and  $\overline{ENT}$  are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Whenever  $\overline{ENP}$  and/or  $\overline{ENT}$  is taken high,  $\overline{RCO}$  either goes high or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The 74ACT11867 is characterized for operation from -40°C to 85°C.

DW PACKAGE  
(TOP VIEW)



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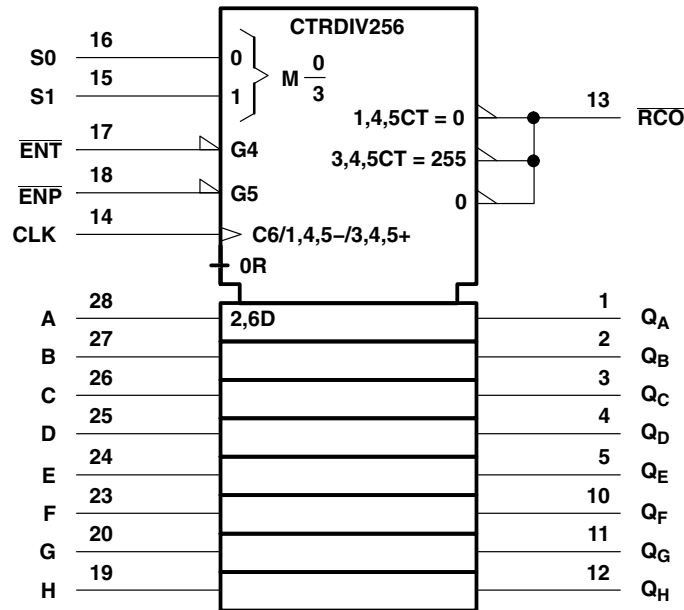
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**MODE FUNCTION TABLE**

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

logic symbol†

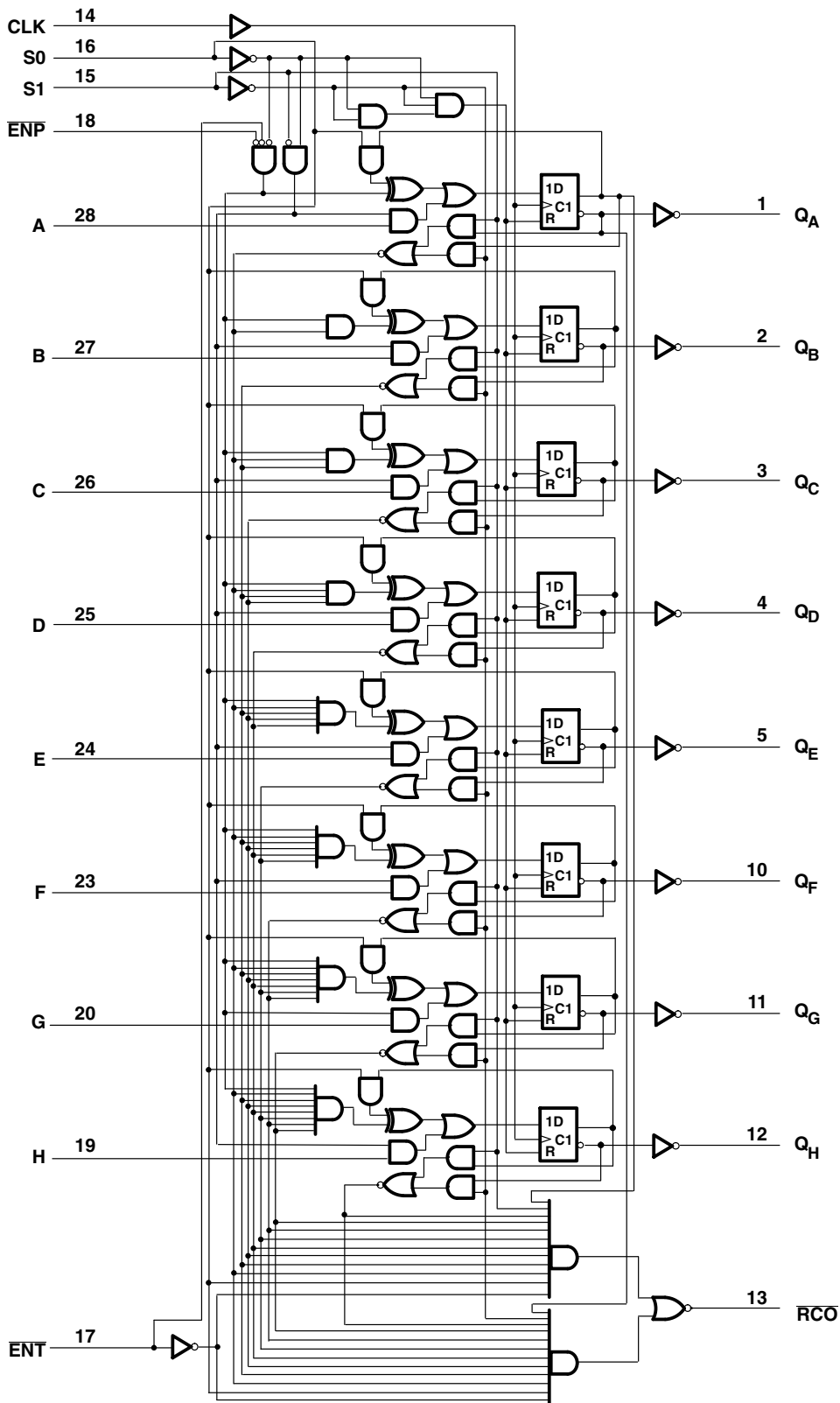


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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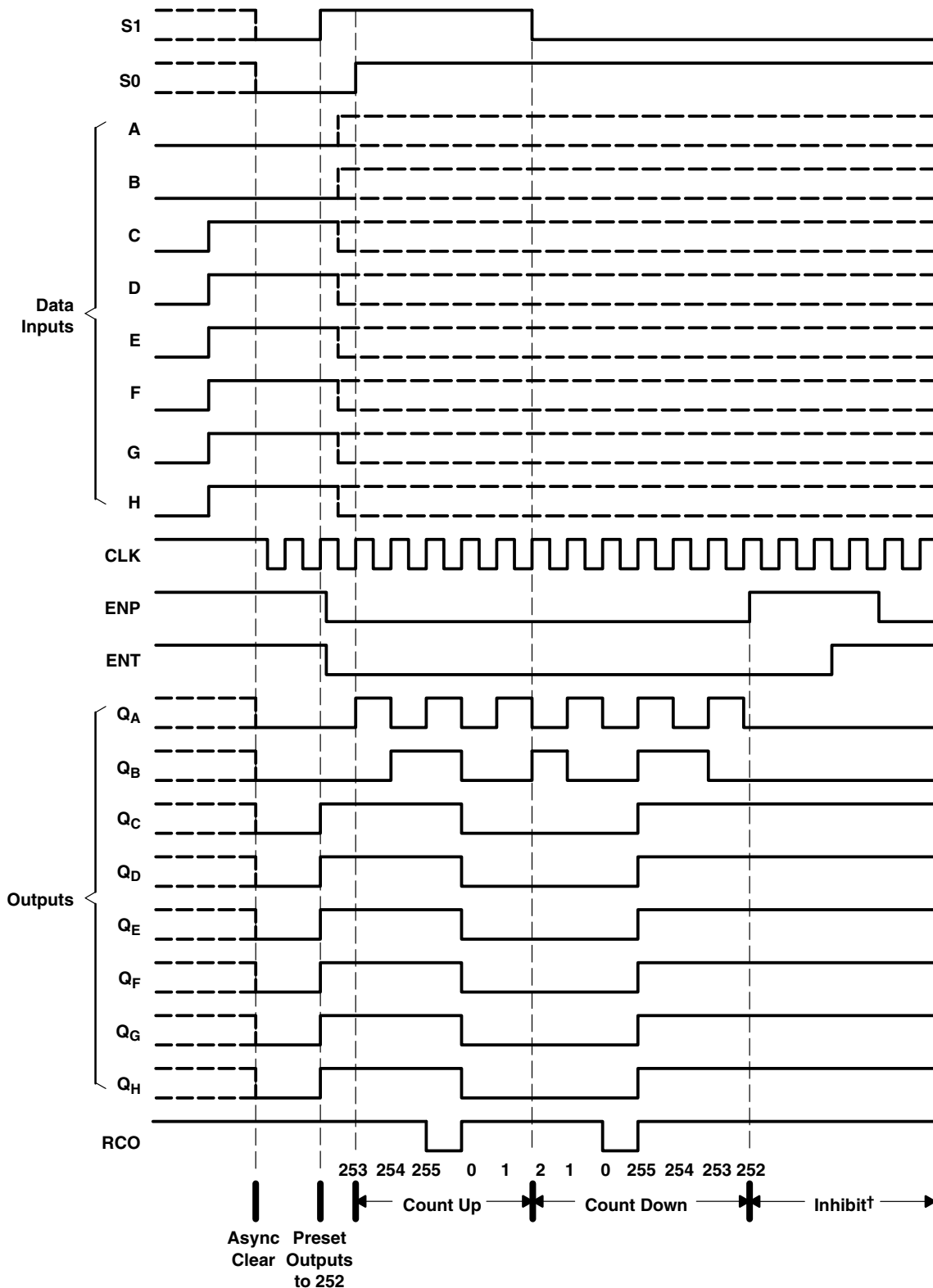
logic diagram (positive logic)



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## output sequence



† ENT and ENP must both be low for counting to occur.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±225 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	78°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 3)**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$I_{OH}$	High-level output current			–24	mA
$I_{OL}$	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$T_A$	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	0.1			0.1		V
		5.5 V	0.1			0.1		
	I <sub>OL</sub> = 24 mA	4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			80		μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V	0.9			1		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5					pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	70	0	70	MHz
t <sub>w</sub>	Pulse duration	S0 and S1 low	12	12		ns
		CLK	6.5	6.5		
t <sub>su</sub> <sup>§</sup>	Setup time before CLK <sup>↑</sup>	Data	8	8		ns
		ENP, ENT	4	4		
		S0, S1 (load)	11	11		
		S0, S1 (count down)	11	11		
		S0, S1 (count up)	11	11		
t <sub>h</sub>	Hold time after CLK <sup>↑</sup>	Data	1	1		ns
t <sub>skew</sub>	Skew time between S0 and S1 to avoid inadvertent clear <sup>¶</sup>	S0 and S1 low	0	0		ns

<sup>§</sup> This setup time is required to ensure stable data.

<sup>¶</sup> This is the maximum time for which S0 and S1 can be low simultaneously when the device transitions between the load (S1 = H, S0 = L) and count-down (S1 = L, S0 = H) modes.



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			70			70		MHz
$t_{\text{PLH}}$	CLK	$\overline{\text{RCO}}$	6	9.9	12.7	6	14.6	ns
$t_{\text{PHL}}$			6.4	10.9	14.2	6.4	16.3	
$t_{\text{PLH}}$	CLK	Q	5	8.9	11.9	5	13.6	ns
$t_{\text{PHL}}$			4.9	9	12.2	4.9	14	
$t_{\text{PLH}}$	ENT	$\overline{\text{RCO}}$	3.9	6.8	9.1	3.9	10.5	ns
$t_{\text{PHL}}$			3.1	7	10.2	3.1	11.5	
$t_{\text{PHL}}$	Clear (S0, S1 low)	Q	6.3	11.9	16.6	6.3	19.1	ns
$t_{\text{PLH}}$	S0, S1 (count up/down)	$\overline{\text{RCO}}$	5.5	10.4	15.6	5.5	17.8	ns
$t_{\text{PHL}}$	S0, S1 (count up/down)	$\overline{\text{RCO}}$	5.6	10.1	14.8	5.6	17.2	ns
$t_{\text{PHL}}$	Clear (S0, S1 low)	$\overline{\text{RCO}}$	6.2	11.3	15.6	6.2	17.8	ns

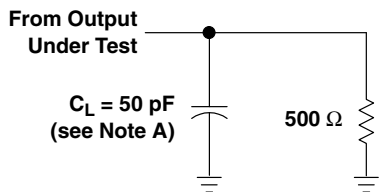
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	62	pF

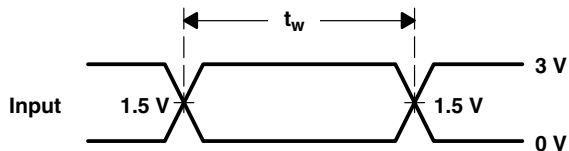
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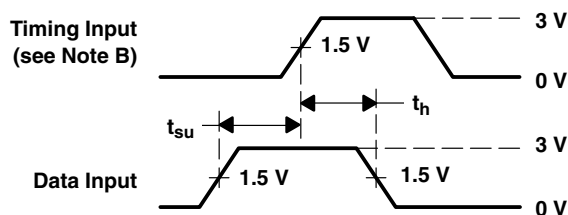
**PARAMETER MEASUREMENT INFORMATION**



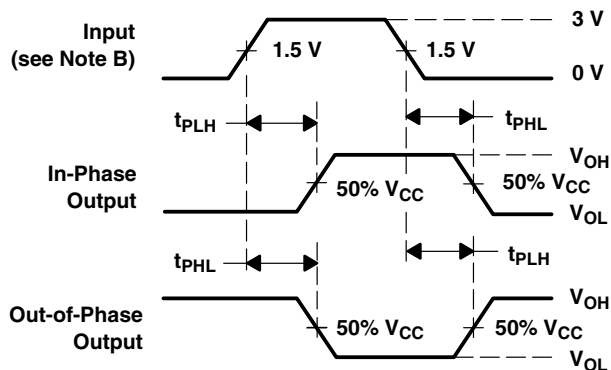
**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS**



**VOLTAGE WAVEFORMS**



**VOLTAGE WAVEFORMS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74ACT11867DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	Samples Not Available
74ACT11867DWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	Samples Not Available
74ACT11867NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

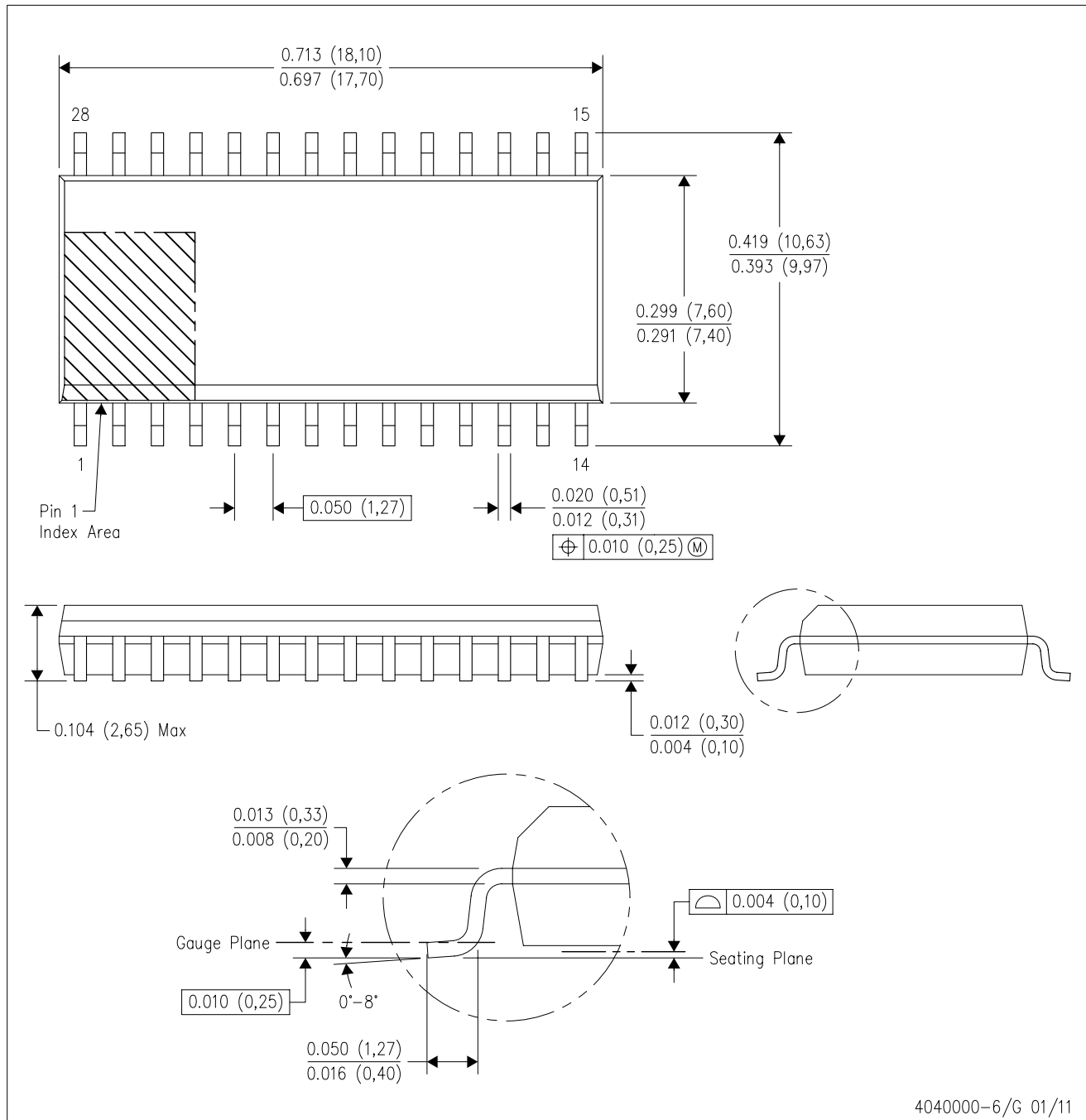
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040000-6/G 01/11

- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

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