54F534,74F534

54F534 74F534 Octal D-Type Flip-Flop with TRI-STATE(RM) Outputs

TEXAS
INSTRUMENTS

Literature Number: SNOS201A

N *a t i o n a l   S e m i c o n d u c t o r*

May 1995

54F/74F534
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'F534 is a high speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F534PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F534DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F534SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F534SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F534FM (Note 2)	W20A	20-Lead Cerpack
	54F534LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX, and SJX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB
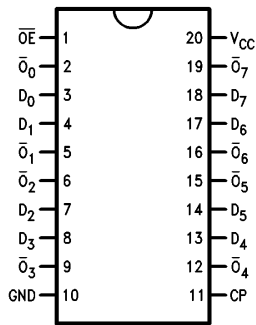
Logic Symbols

TL/F/9549–1

IEEE/IEC

TL/F/9549–5
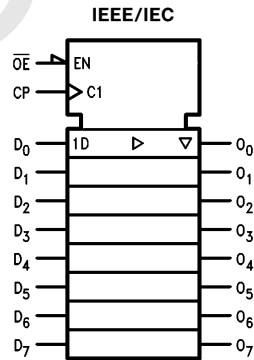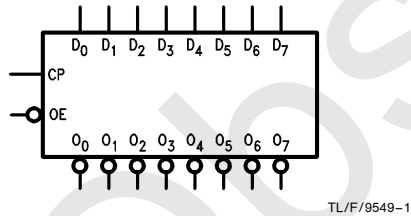
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/$-$0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/$-$0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/$-$0.6 mA
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs	150/40(33.3)	$-$3 mA/24 mA (20 mA)

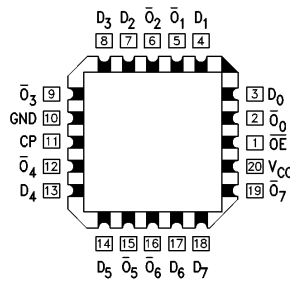TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

```
OE   — 1        20 — VCC
O0   — 2        19 — O7
D0   — 3        18 — D7
D1   — 4        17 — D6
O1   — 5        16 — O6
O2   — 6        15 — O5
D2   — 7        14 — D5
D3   — 8        13 — D4
O3   — 9        12 — O4
GND  — 10       11 — CP
```

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Pin Assignment for LCC

```
        D3  D2  O2  O1  D1
        8   7   6   5   4

  O3  9                   3  D0
  GND 10                  2  O0
  CP  11                  1  OE
  O4  12                  20 VCC
  D4  13                  19 O7

        14  15  16  17  18
        D5  O5  O6  D6  D7
```
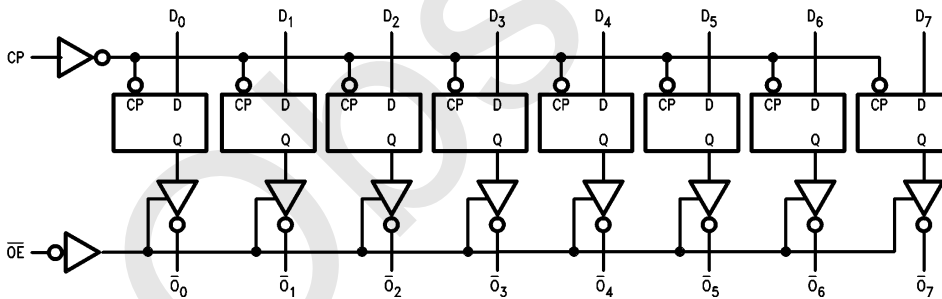
TL/F/9549–3

Functional Description

The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Output
CP	**OE**	**D**	**$\overline{O}$**
⤒	L	H	L
⤒	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⤒ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Logic Diagram

TL/F/9549–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE Output	$-0.5V$ to $+5.5V$

Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		54F 10% V_{CC}	2.4					$I_{OH} = -3$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.4					$I_{OH} = -3$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -3$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 24$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9 \mu$A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 1.50 \mu$A All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OZH}	Output Leakage Current				50	μA	Max	$V_{OUT} = 2.7V$
I_{OZL}	Output Leakage Current				-50	μA	Max	$V_{OUT} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	$V_{OUT} = 5.25V$
I_{CCZ}	Power Supply Current			55	86	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} = $ Mil $C_L = 50$ pF		74F $T_A, V_{CC} = $ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100			60		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.0	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14.0 10.0	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	5.3 4.3	7.0 5.5	1.5 1.5	8.0 7.5	1.5 1.5	8.0 6.5	

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = $ Mil		74F $T_A, V_{CC} = $ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0		2.0 2.5		2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0		2.0 2.5		2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 6.0		7.0 6.0		7.0 6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:
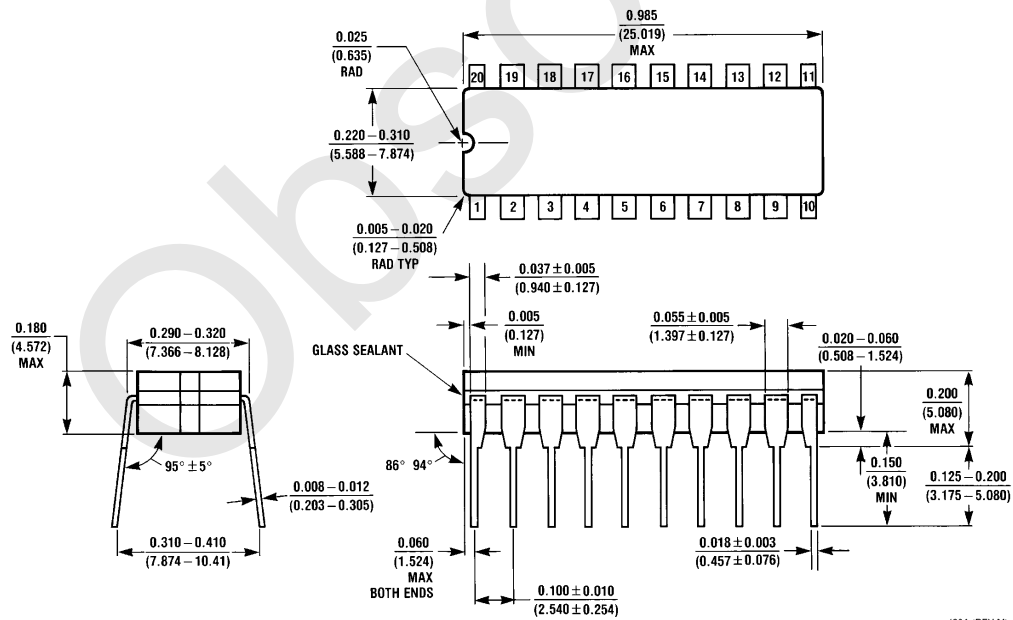
74F 534 S C X

Temperature Range Family —
74F = Commercial
54F = Military

Device Type —

Package Code —
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ

Special Variations
QB = Military grade device with environmental and burn-in processing

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

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Physical Dimensions inches (millimeters)

Top View

Side View

DETAIL A

PIN #1 INDEX

Bottom View

Detail A

E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
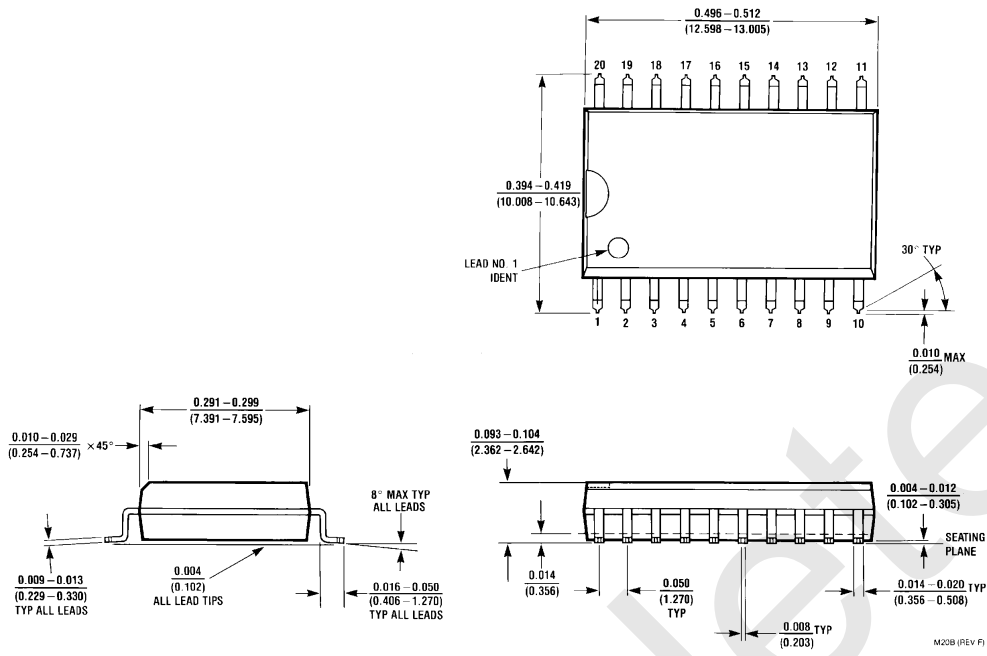**NS Package Number E20A**

GLASS SEALANT

J20A (REV M)

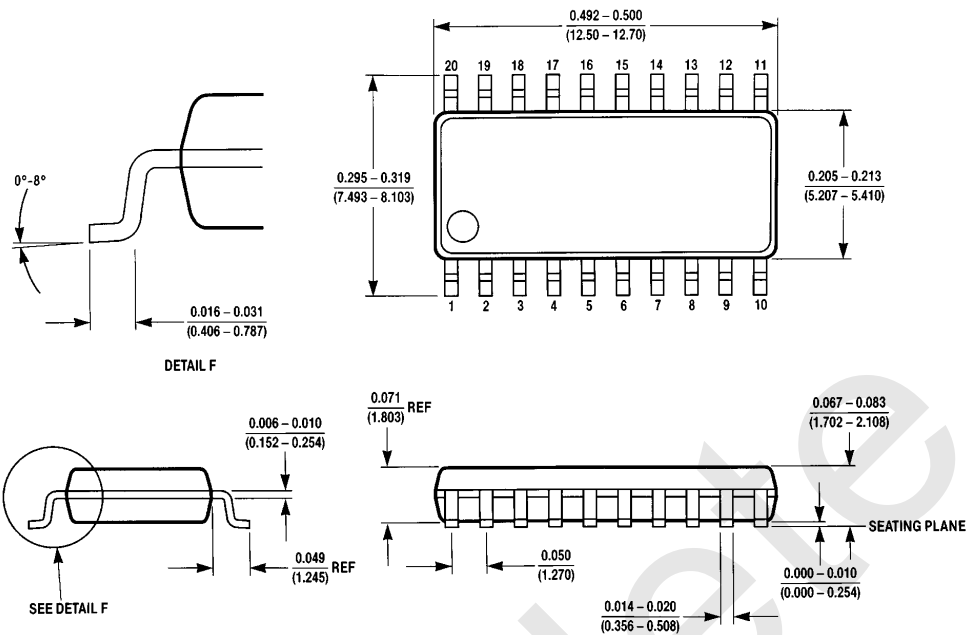**20-Lead Ceramic Dual-In-Line Package (D)**
NS Package Number J20A
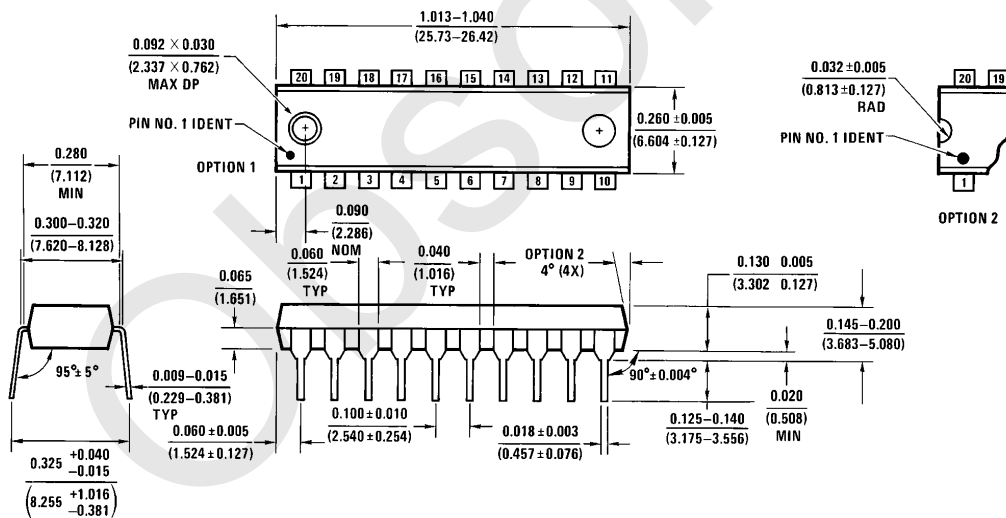
5

Physical Dimensions inches (millimeters) (Continued)

20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
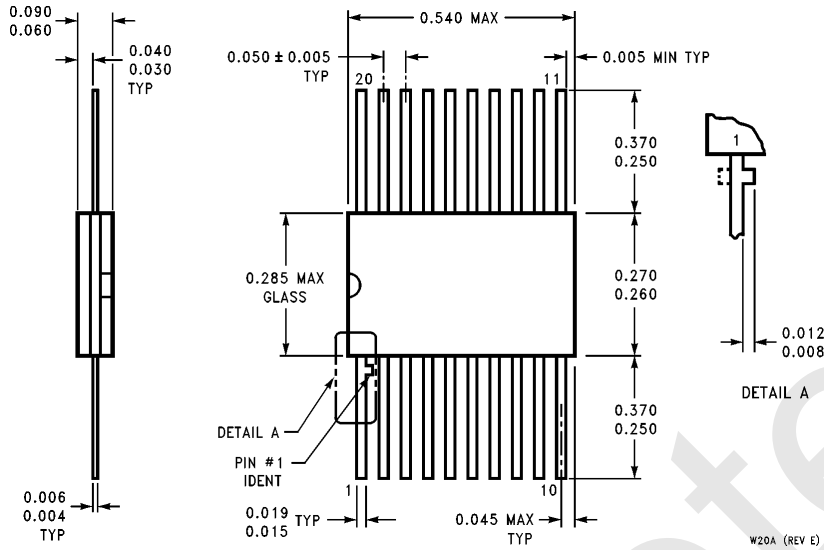**NS Package Number M20B**

Physical Dimensions inches (millimeters) (Continued)

0.492 – 0.500
(12.50 – 12.70)

20 19 18 17 16 15 14 13 12 11

0.295 – 0.319
(7.493 – 8.103)

0.205 – 0.213
(5.207 – 5.410)

1 2 3 4 5 6 7 8 9 10

0°–8°

0.016 – 0.031
(0.406 – 0.787)

DETAIL F

0.006 – 0.010
(0.152 – 0.254)

0.071
(1.803) REF

0.067 – 0.083
(1.702 – 2.108)

SEATING PLANE

SEE DETAIL F

0.049
(1.245) REF

0.050
(1.270)

0.014 – 0.020
(0.356 – 0.508)

0.000 – 0.010
(0.000 – 0.254)

M20D (REV A)

20-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D

1.013–1.040
(25.73–26.42)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

20 19 18 17 16 15 14 13 12 11

PIN NO. 1 IDENT

0.260 ±0.005
(6.604 ±0.127)

OPTION 1

1 2 3 4 5 6 7 8 9 10

0.032 ±0.005
(0.813 ±0.127)
RAD

20 19

PIN NO. 1 IDENT

1

OPTION 2

0.280
(7.112)
MIN

0.300–0.320
(7.620–8.128)

0.090
(2.286)

0.060
(1.524)
NOM

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.130 0.005
(3.302 0.127)

0.065
(1.651)

0.145–0.200
(3.683–5.080)

95°± 5°

0.009–0.015
(0.229–0.381)
TYP

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

90° ±0.004°

0.020
(0.508)

0.060 ±0.005
(1.524 ±0.127)

0.125–0.140
(3.175–3.556)
MIN

0.325 +0.040
−0.015

(8.255 +1.016
−0.381)

N20A (REV G)

20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

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54F/74F534 Octal D-Type Flip-Flop with TRI-STATE Outputs

Physical Dimensions inches (millimeters) (Continued)

0.090
0.060

0.040
0.030
TYP

0.050 ± 0.005
TYP

0.005 MIN TYP

0.540 MAX

20   11

0.370
0.250

0.285 MAX
GLASS

0.270
0.260

0.370
0.250

DETAIL A

PIN #1
IDENT

0.006
0.004
TYP

0.019
0.015
TYP

0.045 MAX
TYP

1   10

0.012
0.008

DETAIL A

W20A (REV E)

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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