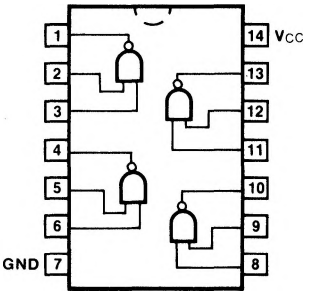
54/7401
54H/74H01

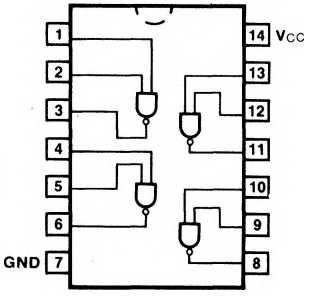
QUAD 2-INPUT NAND GATE
(With Open-Collector Output)

CONNECTION DIAGRAMS

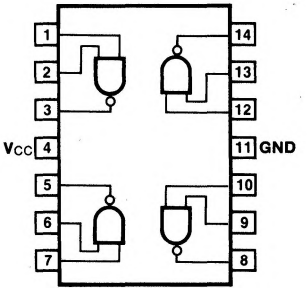
PINOUT A



PINOUT B



PINOUT C



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7401PC		9A
	B	74H01PC		
Ceramic DIP (D)	A	7401DC	5401DM	6A
	B	74H01DC	54H01DM	
Flatpak (F)	C	7401FC, 74H01FC	5401FM, 54H01FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25
Outputs	OC**/10	OC**/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		8.0		10	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		22		40		V_{IN} = Open	
t_{PLH}	Propagation Delay		45		15	ns	Figs. 3-2, 3-4	
t_{PHL}			15		12			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

**OC — Open Collector