

74LCX16244

Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

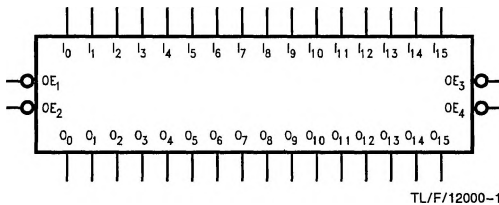
The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16244
- Latch performance exceeds 300 mA
- ESD performance:
 - Human Body Model > 2000V
 - Machine Model > 250V

Ordering Code: See Section 11

Logic Symbol

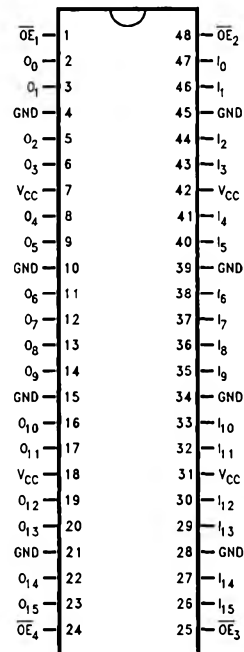


Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16244MEA 74LCX16244MEAX	74LCX16244MTD 74LCX16244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

The LCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE out-

puts are controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
\overline{OE}_1	I ₀ -I ₃	O ₀ -O ₃
L	L	L
L	H	H
H	X	Z

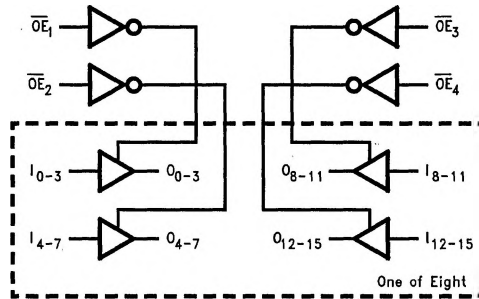
Inputs		Outputs
\overline{OE}_2	I ₄ -I ₇	O ₄ -O ₇
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I ₈ -I ₁₁	O ₈ -O ₁₁
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_4	I ₁₂ -I ₁₅	O ₁₂ -O ₁₅
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagram



TL/F/12000-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_I)	-0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	± 100 mA
Storage Temperature Range (TSTG)	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Supply Voltage	
Operating	2.7V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0V to V_{CC}
Output in "OFF" State	0V to 5.5V
Output Current I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.7V$ to 3.0V	± 12 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
V_{IL}	Low Level Input Voltage	2.7-3.6		0.8		
V_{OH}	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		2.7		2.2		
		3.0		2.4		
		3.0		2.2		
V_{OL}	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		2.7	0.4			
		3.0	0.55			
I_I	Input Leakage Current	2.7-3.6		± 5.0	μA	$0 \leq V_I \leq 5.5V$
I_{OZ}	TRI-STATE Output Leakage	2.7-3.6		± 5.0	μA	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or $V_O = 5.5V$
I_{CC}	Quiescent Supply Current	2.7-3.6		20	μA	$V_I = V_{CC}$ or GND
				± 20	μA	$3.6 \leq (V_I, V_O) \leq 5.5V$
				500	μA	$V_{IH} = V_{CC} - 0.6V$
ΔI_{CC}	Increase in I_{CC} per Input	2.7-3.6			μA	

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Max (Note 2)	
t _{PHL} t _{PHL}	Propagation Delay	2.7 3.0–3.6	1.5 1.5	5.8 5.2	ns
t _{PZL} t _{PZH}	Output Enable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t _{OSSL} t _{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = 25°C	Units	Conditions
			Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	0.8	V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	3.3	0.8	V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance	7	pF	V _{CC} = Open V _I = 0V or V _{CC}
C _{OUT}	Output Capacitance	8	pF	V _{CC} = 3.3V V _I = 0V or V _{CC}
C _{PD}	Power Dissipation Capacitance	32	pF	V _{CC} = 3.3V V _I = 0V or V _{CC} F = 10 MHz