National Semiconductor

PRELIMINARY

74LCX16245
Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

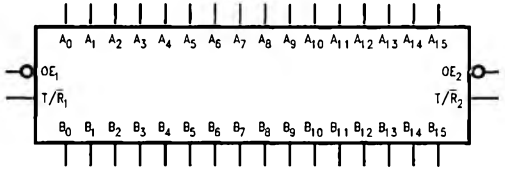
The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Separate control logic for each 8-bit
- Guaranteed simultaneous switching noise level
- Available in SSOP, TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300 mA
- ESD performance:
  Human body model >2000V
  Machine model >250V

Ordering Code: See Section 11

Logic Symbol



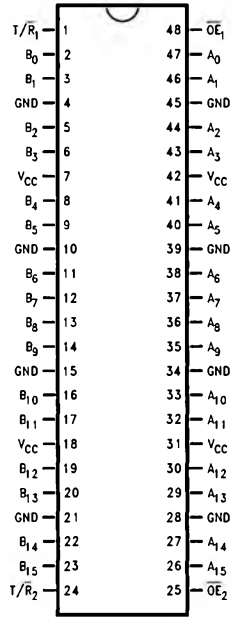
TL/F/12001–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or TRI-STATE Outputs
B_0–B_{15}	Side B Inputs or TRI-STATE Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16245MEA 74LCX16245MEAX	74LCX16245MTD 74LCX16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12001–2

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

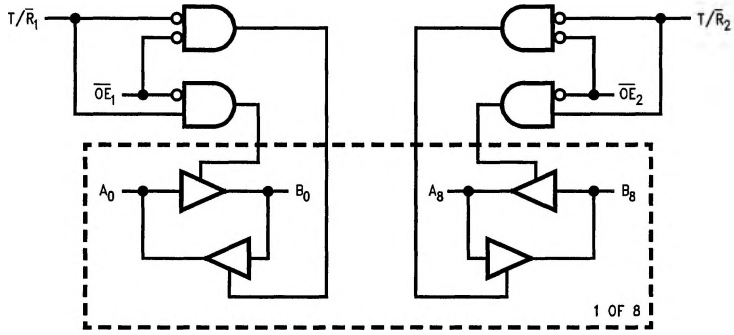
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12001–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) (V_I) < 0	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *I_O Absolute Maximum Rating must be observed.*

Recommended Operating Conditions

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention only	1.5V to 3.6V
Input Voltage (V_I)	0.0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0.0V to V_{CC}
Output in "OFF" State	0.0V to 5.5V
Output Current I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	
V_{CC} = 2.7V to 3.0V	
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate $\Delta t/\Delta V$	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7–3.6	2.0		V	V_{OUT} ≤ 0.1V or
V_{IL}	Low Level Input Voltage	2.7–3.6		0.8		≥ V_{CC} − 0.1V
V_{OH}	High Level Output Voltage	2.7–3.6	V_{CC}−0.2		V	I_{OH} = −100 μA
		2.7	2.2			I_{OH} = −12 mA
		3.0	2.4			I_{OH} = −18 mA
		3.0	2.2			I_{OH} = −24 mA
V_{OL}	Low Level Output Voltage	2.7–3.6		0.2	V	I_{OL} = 100 μA
		2.7		0.4		I_{OL} = 12 mA
		3.0		0.55		I_{OL} = 24 mA
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$	2.7–3.6		±5.0	μA	0 ≤ V_I ≤ 5.5V
I_{OZ}	TRI-STATE I/O Leakage	2.7–3.6		±5.0	μA	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or V_O = 5.5V
I_{CC}	Quietscent Supply Current	2.7–3.6		20	μA	V_I = V_{CC} or GND
				±20	μA	3.6 ≤ (V_I, V_O) ≤ 5.5V
ΔI_{CC}	Increase in I_{CC} per Input	2.7–3.6		500	μA	V_{IH} = V_{CC} −0.6V

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = +40°C$ to $+85°$ C, $C_L = 50$ pF		Units
			Min	Max (Note 2)	
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	2.7 3.0–3.6	1.5 1.5	5.8 5.2	ns
t_{PZL}, t_{PZH}	Output Enable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t_{PHZ}, t_{PLZ}	Output Disable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typical	Units	Conditions
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C_{IN}	Input Capacitance	7	pF	V_{CC} = Open $V_I = 0$V or V_{CC}
$C_{I/O}$	Input/Output Capacitance	8	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC}
C_{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC} F = 10 MHz