National Semiconductor

PRELIMINARY

74LCX16373
Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

The LCX16373 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

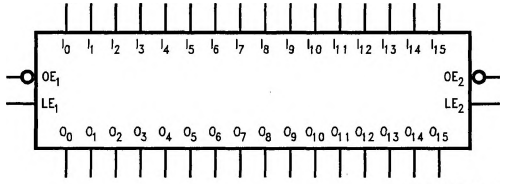
The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latchup performance exceeds 300 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model >250V

Ordering Code: See Section 11

Logic Symbol



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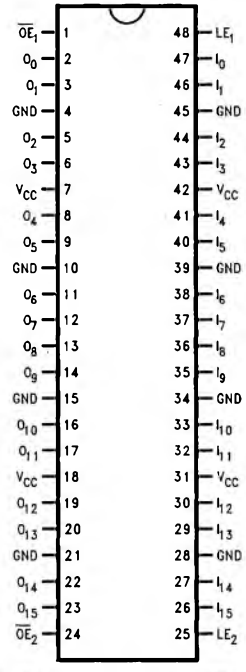
Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16373MEA 74LCX16373MEAX	74LCX16373MTD 74LCX16373MTDX
See NS Package Number	MS48A	MTD48

Conection Diagram

Pin Assignment for SSOP and TSSOP



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Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

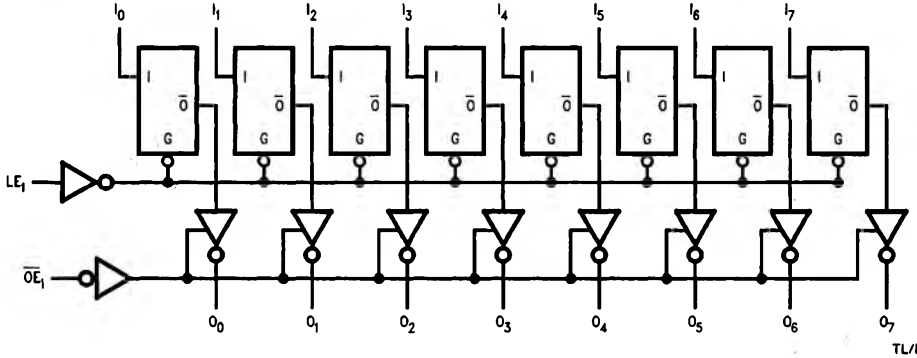
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



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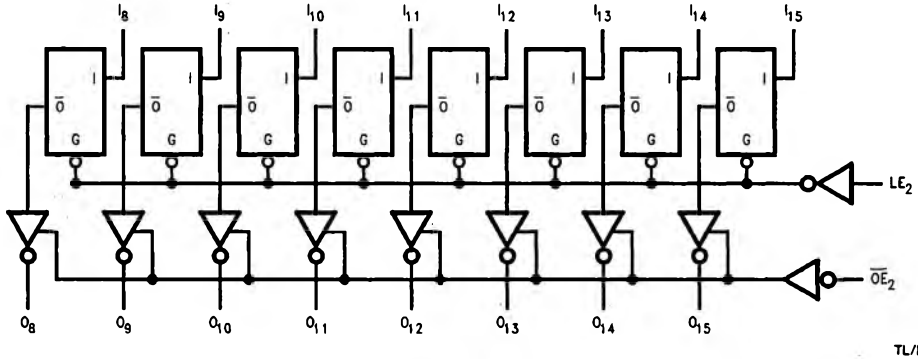

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) $V_I < 0$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0$	−50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *I_O Absolute Maximum Rating must be observed.*

Recommended Operating Conditions

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage (V_I)	0.0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0.0V to V_{CC}
Output in "OFF" State	0.0V to 5.5V
Output Current I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.7V to 3.0V	±12 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7–3.6	2.0		V	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$
V_{IL}	Low Level Input Voltage	2.7–3.6		0.8	V	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$
V_{OH}	High Level Output Voltage	2.7–3.6	$V_{CC} - 0.2$		V	I_{OH} = −100 μA
		2.7	2.2		V	I_{OH} = −12 mA
		3.0	2.4		V	I_{OH} = −18 mA
		3.0	2.2		V	I_{OH} = −24 mA
V_{OL}	Low Level Output Voltage	2.7–3.6		0.2	V	I_{OL} = 100 μA
		2.7		0.4	V	I_{OL} = 12 mA
		3.0		0.55	V	I_{OL} = 24 mA
I_I	Input Leakage Current	2.7–3.6		±5.0	μA	$0 \le V_I \le 5.5V$
I_{OZ}	TRI-STATE Output Leakage	2.7–3.6		±5.0	μA	$0 \le V_O \le 5.5V$, $V_I = V_{IH}$ or V_{IL}
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or V_O = 5.5V
I_{CC}	Quiescent Supply Current	2.7–3.6		20	μA	$V_I = V_{CC}$ or GND
				±20	μA	$3.6 \le (V_I, V_O) \le 5.5V$
ΔI_{CC}	Increase in I_{CC} per Input	2.7–3.6		500	μA	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Max (Note 2)	
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to Output	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t_S	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t_H	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t_W	Clock Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typical	Units	Conditions
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C_{IN}	Input Capacitance	7	pF	V_{CC} = Open $V_I = 0$V or V_{CC}
C_{OUT}	Output Capacitance	8	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC}
C_{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC} F = 10 MHz