

54S/74S258
54LS/74LS258

QUAD 2-INPUT MULTIPLEXER
 (With 3-State Outputs)

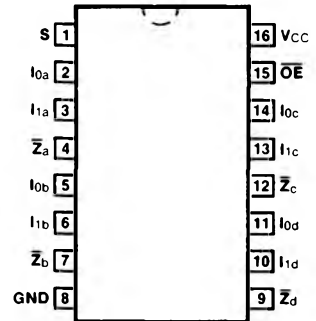
DESCRIPTION — The '258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- INVERTING 3-STATE OUTPUTS

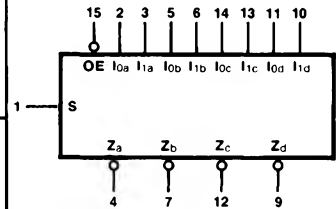
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74S258PC, 74LS258PC		9B
Ceramic DIP (D)	A	74S258DC, 74LS258DC	54S258DM, 54LS258DM	6B
Flatpak (F)	A	74S258FC, 74LS258FC	54S258FM, 54LS258FM	4L

CONNECTION DIAGRAM
 PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
 GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S	Common Data Select Input	2.5/2.5	1.0/0.5
OE	3-State Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
I _{0a} — I _{0d}	Data Inputs from Source 0	1.25/1.25	0.5/0.25
I _{1a} — I _{1d}	Data Inputs from Source 1	1.25/1.25	0.5/0.25
Z̄ _a — Z̄ _d	Inverting Data Outputs	162/12.5 (50)	65/15 (25)/(7.5)

FUNCTIONAL DESCRIPTION — This device is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{aligned}\bar{Z}_a &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) & \bar{Z}_b &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Z}_c &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) & \bar{Z}_d &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})\end{aligned}$$

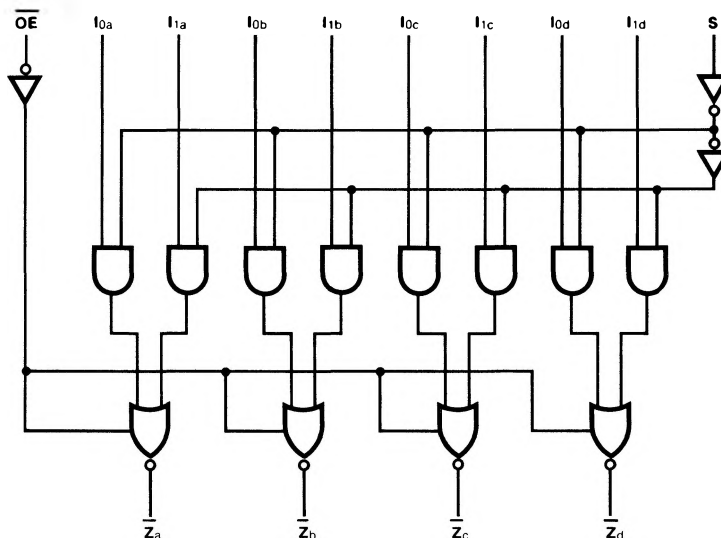
When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
\overline{OE}	S	I_0	I_1	\bar{Z}
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-40	-100	-20	-100	mA	$V_{CC} = \text{Max}$
I_{CC}	Power Supply Current	Outputs HIGH		7.0		mA	$V_{CC} = \text{Max}; S, I_{1x} = 4.5 \text{ V}$ $\overline{OE}, I_{0x} = \text{Gnd}$
		Outputs LOW		14			$V_{CC} = \text{Max}; I_{1x} = 4.5 \text{ V}$ $\overline{OE}, I_{0x}, S = \text{Gnd}$
		Outputs OFF		19			$V_{CC} = \text{Max}; S, I_{0x} = \text{Gnd}$ $\overline{OE} = I_{1x} = 4.5 \text{ V}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{ C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	6.0		18		ns	Figs. 3-1, 3-4
		6.0		18			
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	12		21		ns	Figs. 3-1, 3-4
		12		21			
t_{PZH} t_{PZL}	Output Enable Time	19.5		30		ns	Figs. 3-3, 3-11, 3-12 $R_L = 2 \text{ k}\Omega$ ('LS258)
		21		30			
t_{PHZ} t_{PLZ}	Output Disable Time	8.5		30		ns	Figs. 3-3, 3-11, 3-12 $R_L = 2 \text{ k}\Omega$, $C_L = 5 \text{ pF}$ ('LS258)
		14		25			