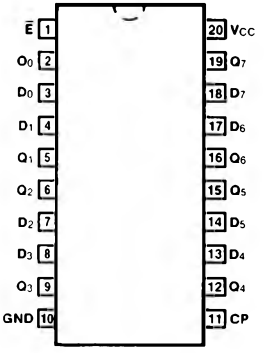
54LS/74LS377

OCTAL D FLIP-FLOP

(With Common Enable and Clock)

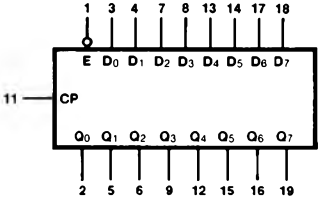
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

- **8-BIT HIGH SPEED PARALLEL REGISTERS**
- **POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOPS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS377PC		9Z
Ceramic DIP (D)	A	74LS377DC	54LS377DM	4E
Flatpak (F)	A	74LS377FC	54LS377FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.25
D_0 — D_7	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q_0 — Q_7	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

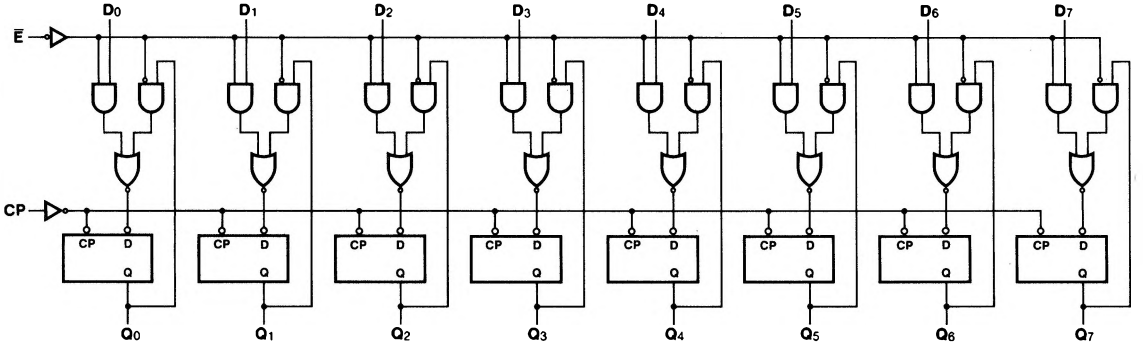
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	X	X	No change
L	⎍⎍	H	H
L	⎍⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		28	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		25 25	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	10 20		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20		ns	Fig. 3-8