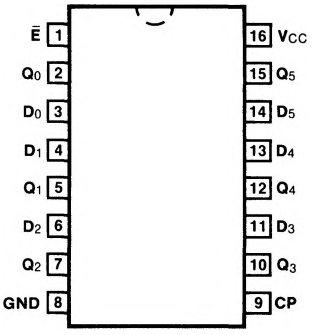
54LS/74LS378

PARALLEL D REGISTER

(With Enable)

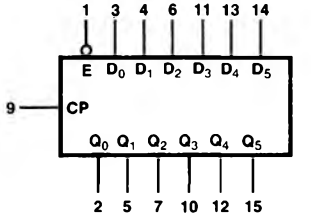
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '378 is a 6-bit register with a buffered common enable. This device is similar to the '174, but with common Enable rather than common Master Reset.

- **6-BIT HIGH SPEED PARALLEL REGISTER**
- **POSITIVE EDGE-TRIGGERED D-TYPE INPUTS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULL TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS378PC		9B
Ceramic DIP (D)	A	74LS378DC	54LS378DM	6B
Flatpak (F)	A	74LS378FC	54LS378FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
Ē	Enable Input (Active LOW)	0.5/0.25
D0 — D5	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q0 — Q5	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

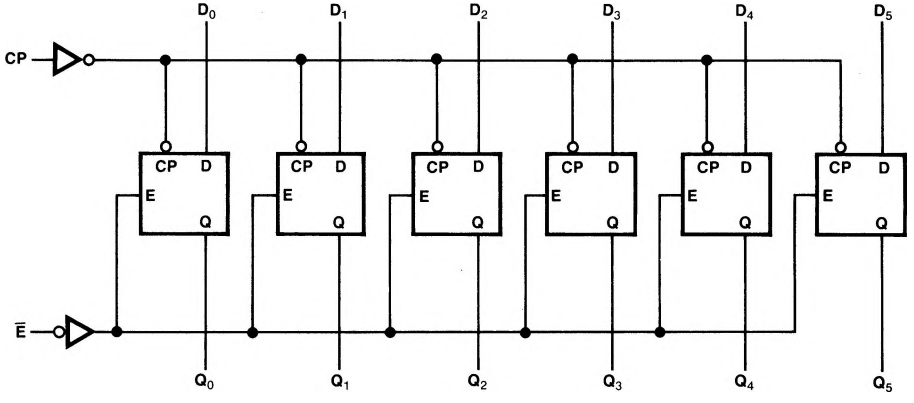
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	⎍	X	No change
L	⎍	H	H
L	⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		22	mA	V_{CC} = Max, D_n = $\overline{E}$ = Gnd CP = ⎍⎾

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, D_n to CP	20		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_n to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D_n to CP	20		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_n to CP	5.0		ns	Fig. 3-6
t_s (H)	Setup Time HIGH, $\overline{E}$ to CP	30		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, $\overline{E}$ to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, $\overline{E}$ to CP	30		ns	Fig. 3-6
t_h (L)	Hold Time LOW, $\overline{E}$ to CP	5.0		ns	Fig. 3-6
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8