

# 54LS/74LS573

## OCTAL D-TYPE LATCH

(With 3-State Outputs)

**DESCRIPTION** — The '573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

This device is functionally identical to the 'LS373, but has different pinouts. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet.

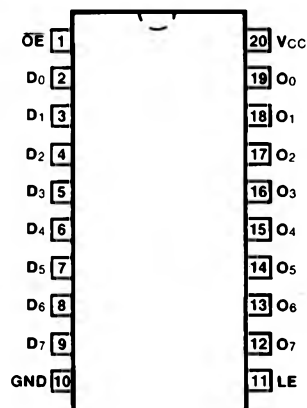
- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS373**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

**ORDERING CODE:** See Section 9

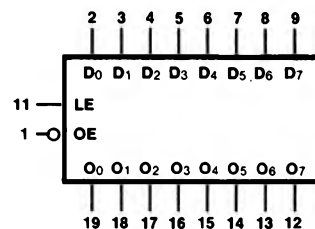
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS573PC		9Z
Ceramic DIP (D)	A	74LS573DC	54LS573DM	4E
Flatpak (F)	A	74LS573FC	54LS573FM	4F

### CONNECTION DIAGRAM

#### PINOUT A



### LOGIC SYMBOL



$V_{CC} = \text{Pin } 20$   
 $\text{Gnd} = \text{Pin } 10$

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D <sub>0</sub> — D <sub>7</sub>	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
O <sub>0</sub> — O <sub>7</sub>	3-State Latch Outputs	65/15 (25)/(7.5)