National Semiconductor

74LVQ00
Low Voltage Quad 2-Input NAND Gate

General Description

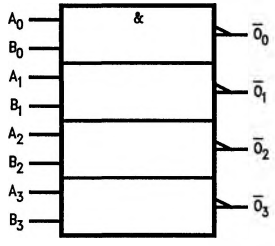
The LVQ00 contains four 2-input NAND gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbol



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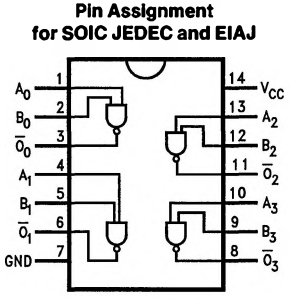
Connection Diagram



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Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ00SC 74LVQ00SCX	74LVQ00SJ 74LVQ00SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ00 T_A = +25°C		74LVQ00 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ00 $T_A = +25°C$		74LVQ00 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0		V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−1.0		V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ00 $T_A = +25°C$, $C_L = 50$ pF			74LVQ00 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.7	2.0	8.4	13.4	2.0	14.0	ns
		3.3 ± 0.3	2.0	7.0	9.5	2.0	10.0	
t_{PHL}	Propagation Delay	2.7	1.5	6.6	11.3	1.0	12.0	ns
		3.3 ± 0.3	1.5	5.5	8.0	1.0	8.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ± 0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	22	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.