

# 74LVQ245

## Low Voltage Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

### General Description

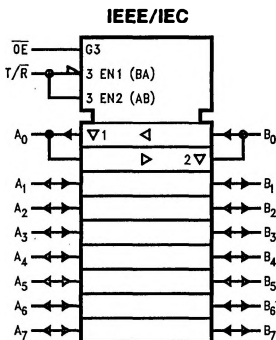
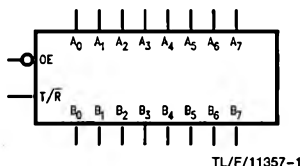
The LVQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 12 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

### Features

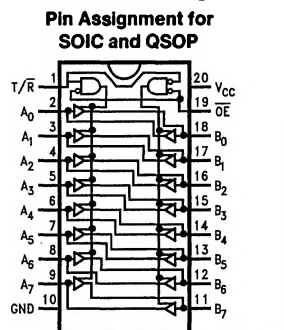
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54 ACQ products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

### Logic Symbols



### Connection Diagram



Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A TRI-STATE Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B TRI-STATE Inputs or TRI-STATE Outputs

### Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ245SC 74LVQ245SCX	74LVQ245SJ 74LVQ245SJX	74LVQ245QSC 74LVQ245QSCX
See NS Package Number	M20B	M20D	MQA20

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±400 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
LVQ	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74LVQ	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	125 mV/ ns

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	74LVQ245		74LVQ245		Units	Conditions
			$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$			
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
$V_{IL}$	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		3.0		2.58	2.48	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 mA$	
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = +12 mA$	
$I_{IN}$	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	$V_I = V_{CC}, GND$	

\*All outputs loaded; thresholds on input associated with output under test.

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ245		74LVQ245		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	† Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			-25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	3.6		±0.3	±3.0		μA	V <sub>I(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.5	-0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ245			74LVQ245		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	2.0 2.0	9.0 7.5	14.0 10.0	2.0 2.0	15.0 10.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	3.0 3.0	10.2 8.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	10.2 8.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 3.3V$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	67	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.