

# 74LVQ273

## Low Voltage Octal D Flip-Flop

### General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

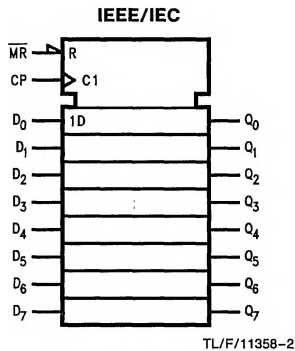
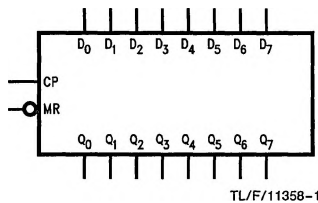
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

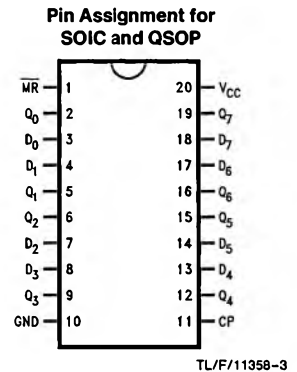
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

### Logic Symbols



### Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ273SC 74LVQ273SCX	74LVQ273SJ 74LVQ273SJX	74LVQ273QSC 74LVQ273QSCX
See NS Package Number	M20B	M20D	MQA20

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±400 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74LVQ	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate $\Delta V/\Delta t$	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

**DC Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	74LVQ273		74LVQ273		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
$V_{IL}$	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		3.0		2.58	2.48	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$	
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$	
$I_{IN}$	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	$V_I = V_{CC}, \text{GND}$	

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273		74LVQ273		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	† Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			-25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.3	-0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273			74LVQ273		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 90			45 75		MHz
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t <sub>PHL</sub>	Propagation Delay M̄R to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
t <sub>OSSL</sub>	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
t <sub>OSLH</sub>		3.3 ± 0.3		1.0	1.5		1.5	

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

**AC Operating Requirements:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273		74LVQ273		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3		6.5 5.0	8.5 6.0	ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3		0.0 0.0	0.0 0.0	ns	
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	2.7 3.3 ± 0.3		7.0 5.5	8.5 6.0	ns	
t <sub>w</sub>	MR Pulse Width HIGH or LOW	2.7 3.3 ± 0.3		7.0 5.5	8.5 6.0	ns	
t <sub>w</sub>	Recovery Time MR to CP	2.7 3.3 ± 0.3		5.0 4.0	6.5 4.5	ns	

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	35	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.