National Semiconductor

ADVANCE INFORMATION

74LVT16373
3.3V ABT 16-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The LVT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

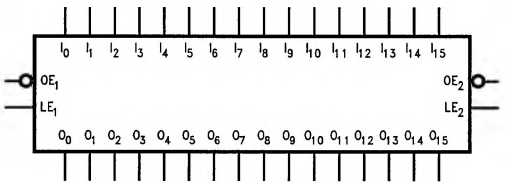
These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



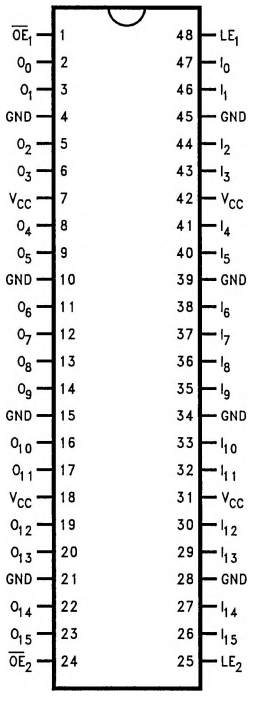
TL/F/12021–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16373MEA 74LVT16373MEAX	74LVT16373MTD 74LVT16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Functional Description

The LVT16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

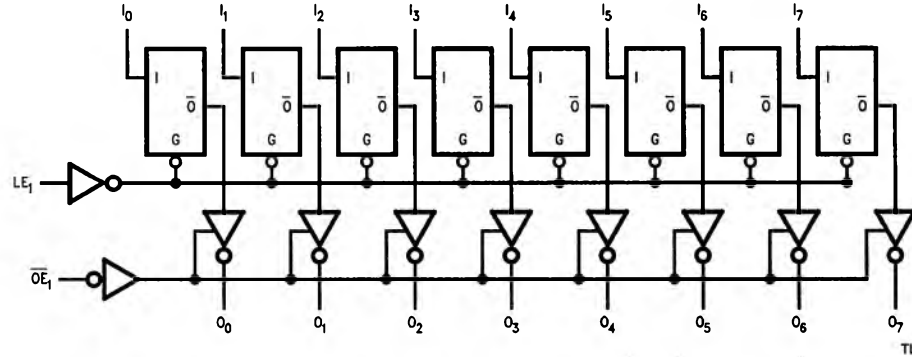
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous output prior to HIGH to LOW transition of LE

Logic Diagrams



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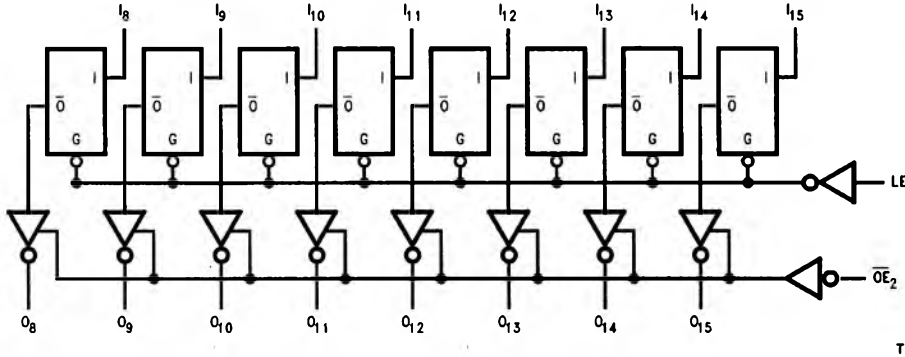

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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.