National Semiconductor

ADVANCE INFORMATION

74LVT16374
3.3V ABT 16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The LVT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

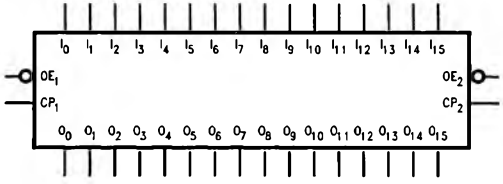
These flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



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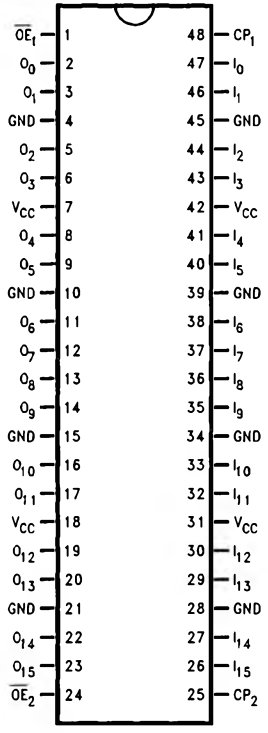
Pin Names	Description
$\overline{OE}_n$	TRI-STATE Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0–I_{15}	Data Inputs
O_0–O_{15}	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16374MEA 74LVT16374MEAX	74LVT16374MTD 74LVT16374MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Functional Description

The LVT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

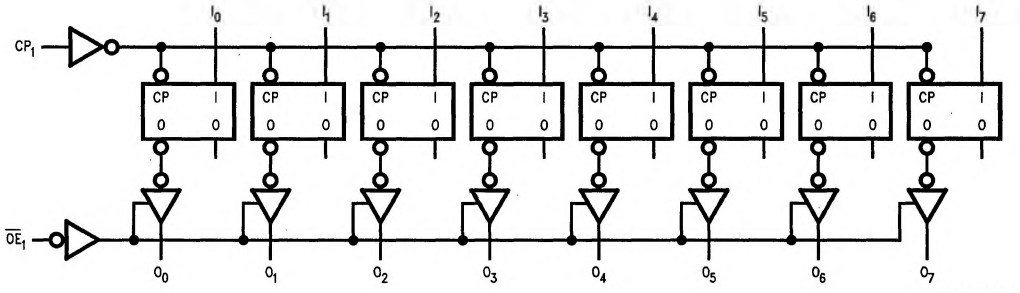
Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagrams

Byte 1 (0:7)



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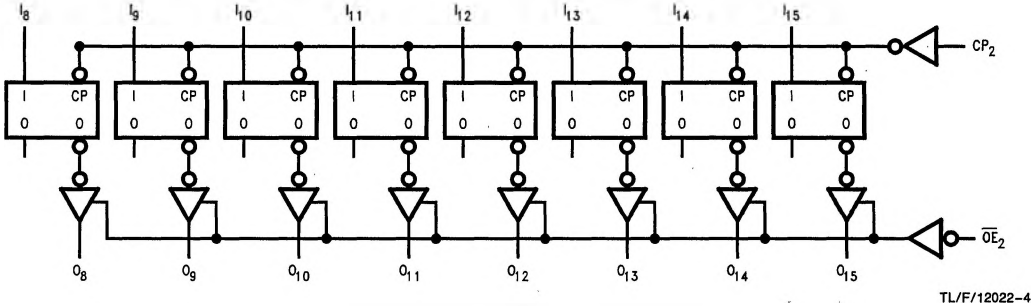
Byte 2 (8:15)



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Please note that these diagrams are provided for the understanding of logic operaiton and should not be used to estimate propagation delays.