National Semiconductor

ADVANCE INFORMATION

74LVT240
3.3V ABT Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

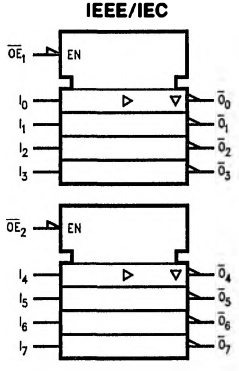
These octal buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



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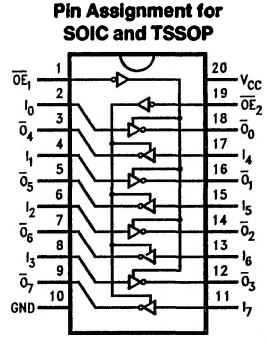
Connection Diagram



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Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT240WM 74LVT240WMX	74LVT240SJ 74LVT240SJX	74LVT240MTCX
See NS Package Number	M20B	M20D	MTC20