



74LVT373

3.3V ABT Octal Transparent Latch with TRI-STATE® Outputs

General Description

The LVT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

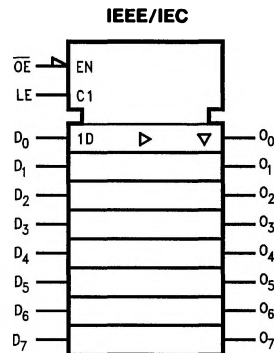
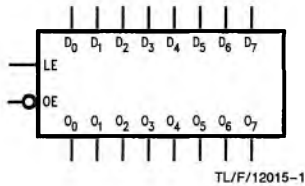
These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

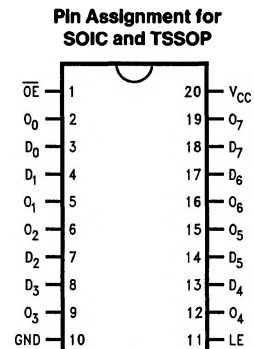
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink $-32\text{ mA}/+64\text{ mA}$
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 373
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbols



Connection Diagram



Pin Names	Description
D_0 - D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
Q_0 - Q_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT373WM 74LVT373WMX	74LVT373SJ 74LVT373SJX	74LVT373MTCX
See NS Package Number	M20B	M20D	MTC20

Functional Description

The LVT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	\overline{OE}	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level

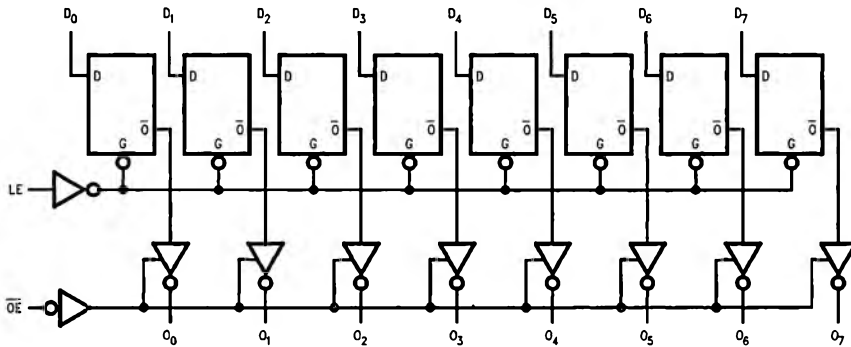
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



TL/F/12015-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.