

## 74LVT373 • 74LVTH373

### Low Voltage Octal Transparent Latch with 3-STATE Outputs

#### General Description

The LVT373 and LVTH373 consist of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus output is in a high impedance state.

The LVTH373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal latches are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 and LVTH373 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

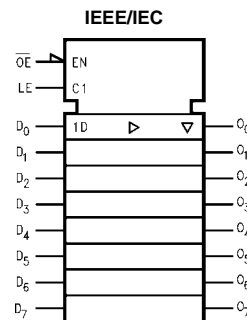
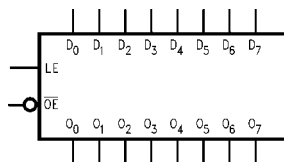
#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH373), also available without bushold feature (74LVT373).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 373

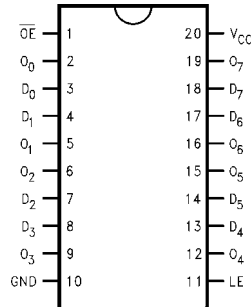
#### Ordering Code:

Order Number	Package Number	Package Description
74LVT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

#### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O <sub>0</sub> –O <sub>7</sub>	3-STATE Latch Outputs

### Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D <sub>n</sub>	O <sub>n</sub>
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O <sub>0</sub>

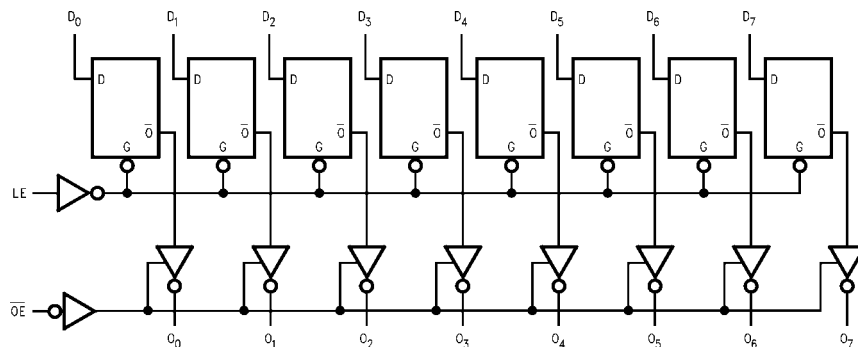
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = High Impedance  
 X = Immaterial  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

### Functional Description

The LVT373 and LVTH373 contain eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preced-

ing the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings <sup>(Note 1)</sup>				
Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 2)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH Level Output Current		-32	mA
$I_{OL}$	LOW Level Output Current		64	mA
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V
<p><b>Note 1:</b> Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p><b>Note 2:</b> <math>I_O</math> Absolute Maximum Rating must be observed.</p>				

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7			-1.2	V	I <sub>I</sub> = -18 mA
V <sub>IH</sub>	Input HIGH Voltage	2.7-3.6	2.0			V	V <sub>O</sub> ≤ 0.1V or
V <sub>IL</sub>	Input LOW Voltage	2.7-3.6			0.8		V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V
V <sub>OH</sub>	Output HIGH Voltage	2.7-3.6	V <sub>CC</sub> - 0.2			V	I <sub>OH</sub> = -100 μA
		2.7	2.4			V	I <sub>OH</sub> = -8 mA
		3.0	2.0			V	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage	2.7			0.2	V	I <sub>OL</sub> = 100 μA
		2.7			0.5	V	I <sub>OL</sub> = 24 mA
		3.0			0.4	V	I <sub>OL</sub> = 16 mA
		3.0			0.5	V	I <sub>OL</sub> = 32 mA
		3.0			0.55	V	I <sub>OL</sub> = 64 mA
I <sub>I(HOLD)</sub> (Note 4)	Bushold Input Minimum Drive	3.0	75			μA	V <sub>I</sub> = 0.8V
			-75			μA	V <sub>I</sub> = 2.0V
I <sub>I(OD)</sub> (Note 4)	Bushold Input Over-Drive Current to Change State	3.0	500			μA	(Note 5)
			-500			μA	(Note 6)
I <sub>I</sub>	Input Current	3.6			10	μA	V <sub>I</sub> = 5.5V
		Control Pins	3.6		±1	μA	V <sub>I</sub> = 0V or V <sub>CC</sub>
		Data Pins	3.6		-5	μA	V <sub>I</sub> = 0V
					1	μA	V <sub>I</sub> = V <sub>CC</sub>
I <sub>OFF</sub>	Power Off Leakage Current	0			±100	μA	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V
I <sub>PU/PD</sub>	Power up/down 3-STATE Output Current	0-1.5V			±100	μA	V <sub>O</sub> = 0.5V to 3.0V V <sub>I</sub> = GND or V <sub>CC</sub>
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6			-5	μA	V <sub>O</sub> = 0.5V
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6			5	μA	V <sub>O</sub> = 3.0V
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6			10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V
I <sub>CCH</sub>	Power Supply Current	3.6			0.19	mA	Outputs HIGH
I <sub>CCL</sub>	Power Supply Current	3.6			5	mA	Outputs LOW
I <sub>CCZ</sub>	Power Supply Current	3.6			0.19	mA	Outputs Disabled
I <sub>CCZ+</sub>	Power Supply Current	3.6			0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 3:** All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

**Note 4:** Applies to Bushold versions only (74LVTH373).

**Note 5:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 6:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 7:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

## Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 9)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 9)

**Note 8:** Characterized in SOIC package. Guaranteed parameter, but not tested.

**Note 9:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50 \text{ pF}, R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 10)	Max	Min	Max	
$t_{PHL}$	Propagation Delay	1.5		4.5	1.5	5.0	ns
$t_{PLH}$	$D_n$ to $O_n$	1.5		4.5	1.5	4.9	
$t_{PHL}$	Propagation Delay	1.7		4.6	1.7	4.9	ns
$t_{PLH}$	LE to $O_n$	1.7		4.5	1.7	5.0	
$t_{PZL}$	Output Enable Time	1.3		4.8	1.3	5.9	ns
$t_{PZH}$		1.3		4.8	1.3	5.5	
$t_{PLZ}$	Output Disable Time	1.9		4.6	1.9	4.9	ns
$t_{PHZ}$		1.9		4.6	1.9	4.9	
$t_W$	LE Pulse Width	3.0			3.0		ns
$t_S$	Setup Time, $D_n$ to LE	1.1			1.0		ns
$t_H$	Hold Time, $D_n$ to LE	1.4			1.4		ns

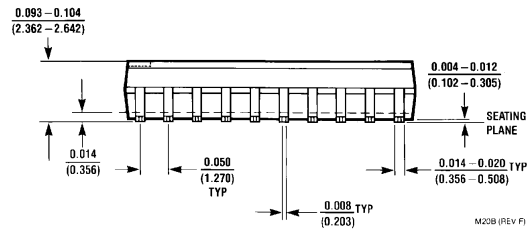
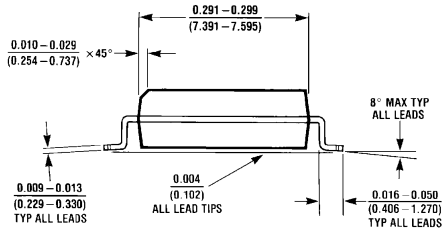
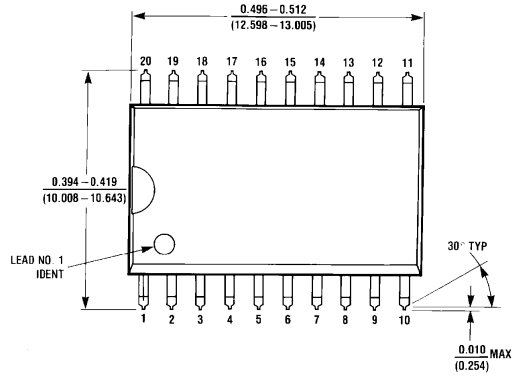
**Note 10:** All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ\text{C}$ .

**Capacitance** (Note 11)

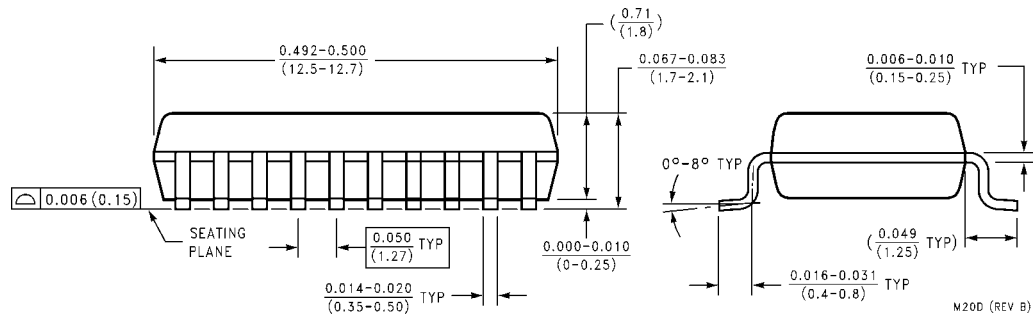
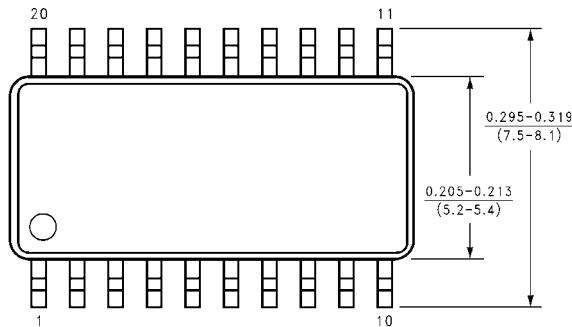
Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}, V_I = 0V \text{ or } V_{CC}$	3	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.0V, V_O = 0V \text{ or } V_{CC}$	5	pF

**Note 11:** Capacitance is measured at frequency  $f = 1 \text{ MHz}$ , per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted

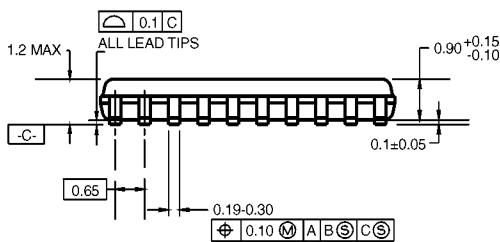
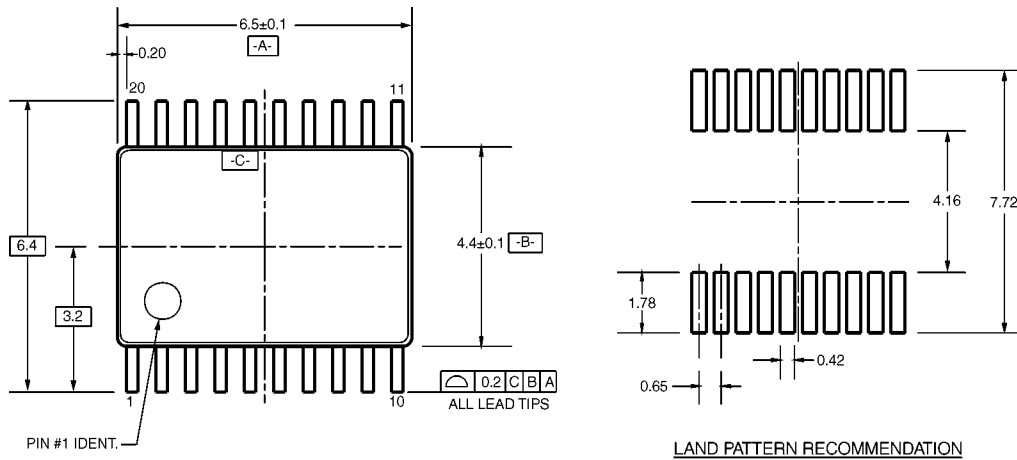


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



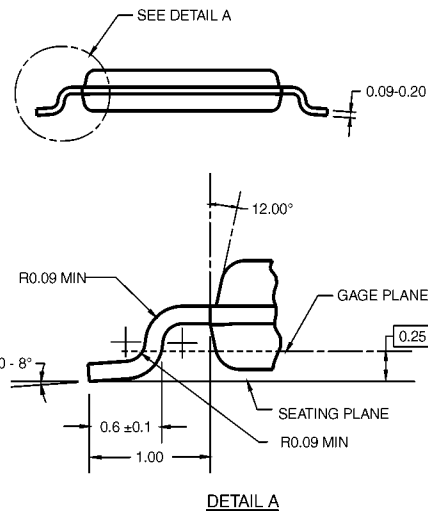
DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**



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