National Semiconductor

74LVX373
Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

General Description

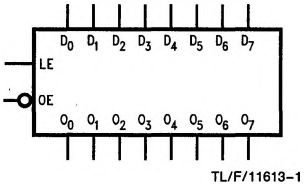
The LVX373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbols



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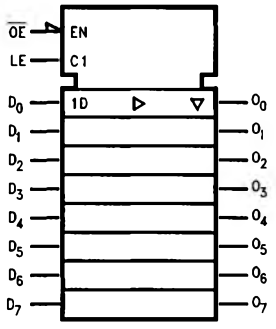
IEEE/IEC



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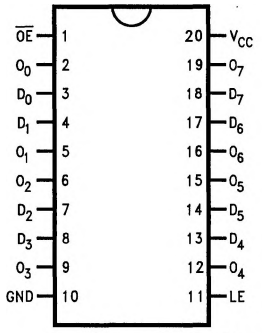
Connection Diagram

Pin Assignment for SOIC and SSOP



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX373M 74LVX373MX	74LVX373SJ 74LVX373SJX	74LVX373MSCX
See NS Package Number	M20B	M20D	MSC20

Functional Description

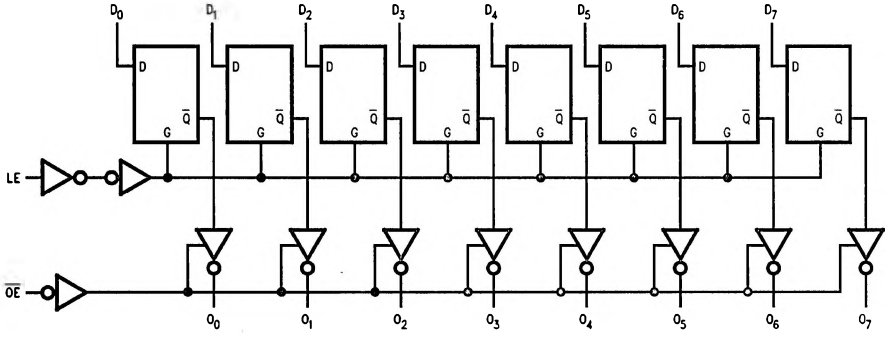
The LVX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX373 T_A = +25°C			74LVX373 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX373 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX373 T_A = +25°C			74LVX373 T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time D_n to O_n	2.7		7.7	15.0	1.0	18.5	ns	C_L = 15 pF
				10.2	18.5	1.0	22.0		C_L = 50 pF
		3.3 ±0.3		6.0	9.7	1.0	11.5		C_L = 15 pF
				8.5	13.2	1.0	15.0		C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time LE to O_n	2.7		7.5	14.5	1.0	17.5	ns	C_L = 15 pF
				10.0	18.0	1.0	21.0		C_L = 50 pF
		3.3 ±0.3		5.8	9.3	1.0	11.0		C_L = 15 pF
				8.3	12.8	1.0	14.5		C_L = 50 pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	2.7		7.7	15.0	1.0	18.5	ns	C_L = 15 pF, R_L = 1 kΩ
				10.2	18.5	1.0	22.0		C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		6.0	9.7	1.0	11.5		C_L = 15 pF, R_L = 1 kΩ
				8.5	13.2	1.0	15.0		C_L = 50 pF, R_L = 1 kΩ
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	2.7		9.8	18.0	1.0	21.0	ns	C_L = 50 pF, R_L = 1 kΩ
		3.3 ±0.3		8.2	12.8	1.0	14.5		C_L = 50 pF, R_L = 1 kΩ
t_W	LE Pulse Width, HIGH	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
t_S	Setup Time, D_n to LE	2.7	6.0			6.0		ns	
		3.3 ±0.3	4.0			4.0			
t_H	Hold Time, D_n to LE	2.7	1.0			1.0		ns	
		3.3 ±0.3	1.0			1.0			
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C_L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX373 $T_A = +25°C$			74LVX373 $T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		27				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per Latch)}}$