National Semiconductor

74LVX74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

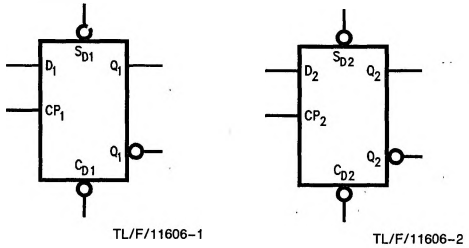
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

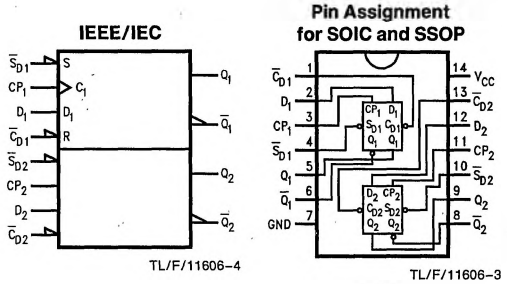
Ordering Code: See Section 11

Logic Symbols



TL/F/11606–1 TL/F/11606–2

Connection Diagram



TL/F/11606–4 TL/F/11606–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐⌐	H	H	L
H	H	⌐⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX74M 74LVX74MX	74LVX74SJ 74LVX74SJX	74LVX74MSCX
See NS Package Number	M14A	M14D	MSC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX74 T_A = +25°C			74LVX74 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX74 T_A = 25°C Typ	74LVX74 T_A = 25°C Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX74 T_A = +25°C Min	Typ	Max	74LVX74 T_A = −40°C to +85°C Min	Max	Units	C_L(pF)
t_{PLH}, t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.7		7.3	15	1.0	18.5	ns	15
				9.8	18.5	1.0	22		50
		3.3 ±0.3		5.7	9.7	1.0	11.5		15
				8.2	13.2	1.0	15		50
t_{PLH}, t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.7		8.4	15.6	1.0	18.5	ns	15
				10.9	19.1	1.0	22		50
		3.3 ±0.3		6.6	10.1	1.0	12		15
				9.1	13.6	1.0	15.5		50
t_W	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	2.7	8.5			10		ns	
		3.3 ±0.3	6			7			
t_S	Setup Time D_n to CP_n	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_H	Hold Time D_n to CP_n	2.7	0.5			0.5		ns	
		3.3 ±0.3	0.5			0.5			
t_{rec}	Recovery Time $\overline{CP}_n$ or $\overline{S}_{Dn}$ to CP_n	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
f_{max}	Maximum Clock Frequency	2.7	55	135		50		MHz	15
			45	60		40			50
		3.3 ±0.3	95	145		80			15
			60	85		50			50
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSLH} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX74			74LVX74		Units
		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		25				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$