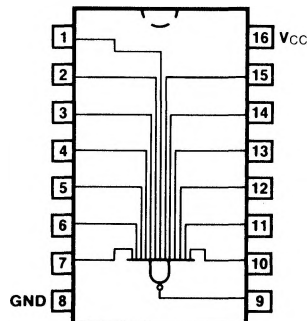


54S/74S133 54LS/74LS133 13-INPUT NAND GATE

**CONNECTION DIAGRAM
PINOUT A**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74S133PC, 74LS133PC		9B
Ceramic DIP (D)	A	74S133DC, 74LS133DC	54S133DM, 54LS133DM	6B
Flatpak (F)	A	74S133FC, 74LS133FC	54S133FM, 54LS133FM	4L



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
I_{CCH}	Power Supply Current	5.0	0.5	10	1.1	mA	$V_{IN} = \text{Gnd}$	$V_{CC} = \text{Max}$
I_{CCL}		$V_{IN} = \text{Open}$						
t_{PLH} t_{PHL}	Propagation Delay	6.0 7.0	15 38			ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{ V}$.