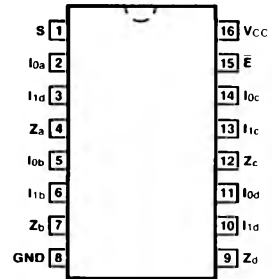


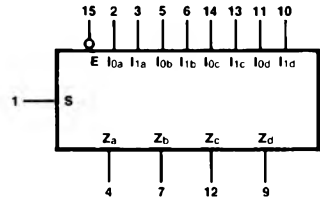
**54/74157**  
**54S/74S157**  
**54LS/74LS157**

**QUAD 2-INPUT MULTIPLEXER**

**CONNECTION DIAGRAM**  
**PINOUT A**



**LOGIC SYMBOL**



VCC = Pin 16  
 GND = Pin 8

**DESCRIPTION** — The '157 is a high speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The '157 can also be used to generate any four of the 16 different functions to two variables.

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74157PC, 74S157PC 74LS157PC		9B
Ceramic DIP (D)	A	74157DC, 74S157DC 74LS157DC	54157DM, 54S157DM 54LS157DM	6B
Flatpak (F)	A	74157FC, 74S157FC 74LS157FC	54157FM, 54S157FM 54LS157FM	4L

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

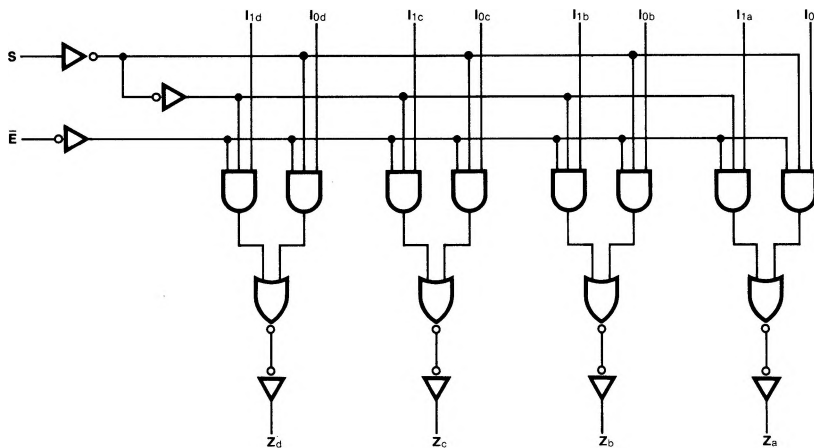
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I0a — I0d	Source 0 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
I1a — I1d	Source 1 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
E	Enable Input (Active LOW)	1.0/1.0	2.5/2.5	1.0/0.5
S	Select Input	1.0/1.0	2.5/2.5	1.0/0.5
Za — Zd	Outputs	20/10	25/12.5	10/5.0 (2.5)

**FUNCTIONAL DESCRIPTION** — The '157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The '157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

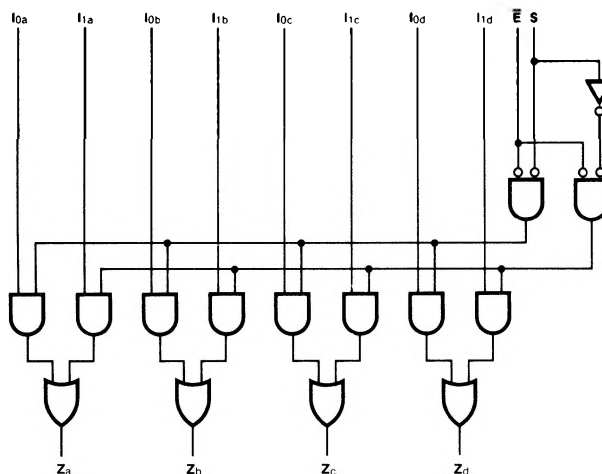
$$\begin{aligned} Z_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) & Z_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) & Z_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

A common use of the '157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The '157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

### LOGIC DIAGRAMS '157



### 'S157 • 'LS157



TRUTH TABLE

INPUTS				OUTPUT
$\bar{E}$	S	I <sub>0</sub>	I <sub>1</sub>	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max			
I <sub>OS</sub>	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V <sub>CC</sub> = Max
		XC	-18	-55	-40	-100	-20	-100		
I <sub>CC</sub>	Power Supply Current	48		78		16		mA	V <sub>CC</sub> = Max All Inputs = 4.5V	

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 15 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>	23 27		15 15		26 24		ns	Figs. 3-1, 3-20
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\bar{E}$ to Z <sub>n</sub>	20 21		12.5 12		20 21		ns	Figs. 3-1, 3-4
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	14 14		7.5 6.5		14 14		ns	Figs. 3-1, 3-5