## DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications.

The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line ( $D$ ) is utilized as an inhibit to allow use in larger decoding networks.

The 8251 and 8252 convert a 4 line input code (with

## LOGIC DIAGRAMS

## TRUTH TABLE

| INPUT STATE |  |  |  | OUTPUT STATES |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 8250 |  |  |  |  |  |  |  | 8251 |  | 8252 |  |
| A | B | C | D | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 8 | 9 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1. | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

## ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | A | B | C | D | OUTPUTS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS |  |  |  |  |  |  |
| "1" Output Voltage | 2.6 | 3.5 |  | V |  |  |  |  | -800 | 6, 10 |
| '00' Output Voltage |  |  | 0.4 | v |  |  |  |  | 16mA | 7, 10 |
| $A, B, C, D$ |  |  | 40 | $\mu \mathrm{A}$ | 4.5 V | 4.5V | 4.5V | 4.5V |  |  |
| " 0 " ${ }^{\prime \prime}$ Input Current A, B, C $(8250,8251)$ | -0.1 |  | -1.2 | mA | 0.4V | 0.4V | 0.4V |  |  |  |
| A, B, C, D (8252) | -0.1 |  | -1.6 | mA | 0.4 V | 0.4 V | 0.4 V | 0.4 V |  |  |
| D (8251 Only) | -0.1 |  | -1.2 | mA |  |  |  | 0.4 V |  |  |
| D (8250 Only) | -0.1 |  | -1.0 | mA |  |  |  | 0.4 V |  |  |

## $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$



## NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
"UP" Level = "1". "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$.
8. Refer to AC Test Figures.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Inputs for " 1 " and " 0 " output voltage test is per TRUTH table with threshold levels of 0.8 V for logical " 0 " and 2.0 V for logical " 1 ".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. $\quad V_{C C}=5.25$ volts.

## SCHEMATIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS



FIGURE 1


FIGURE 2

## TYPICAL APPLICATIONS



## ONE-OF-64 DECODER



