REFER TO PAGE 14 FOR P, N AND Y PACKAGE PIN CONFIGURATIONS.

DESCRIPTION

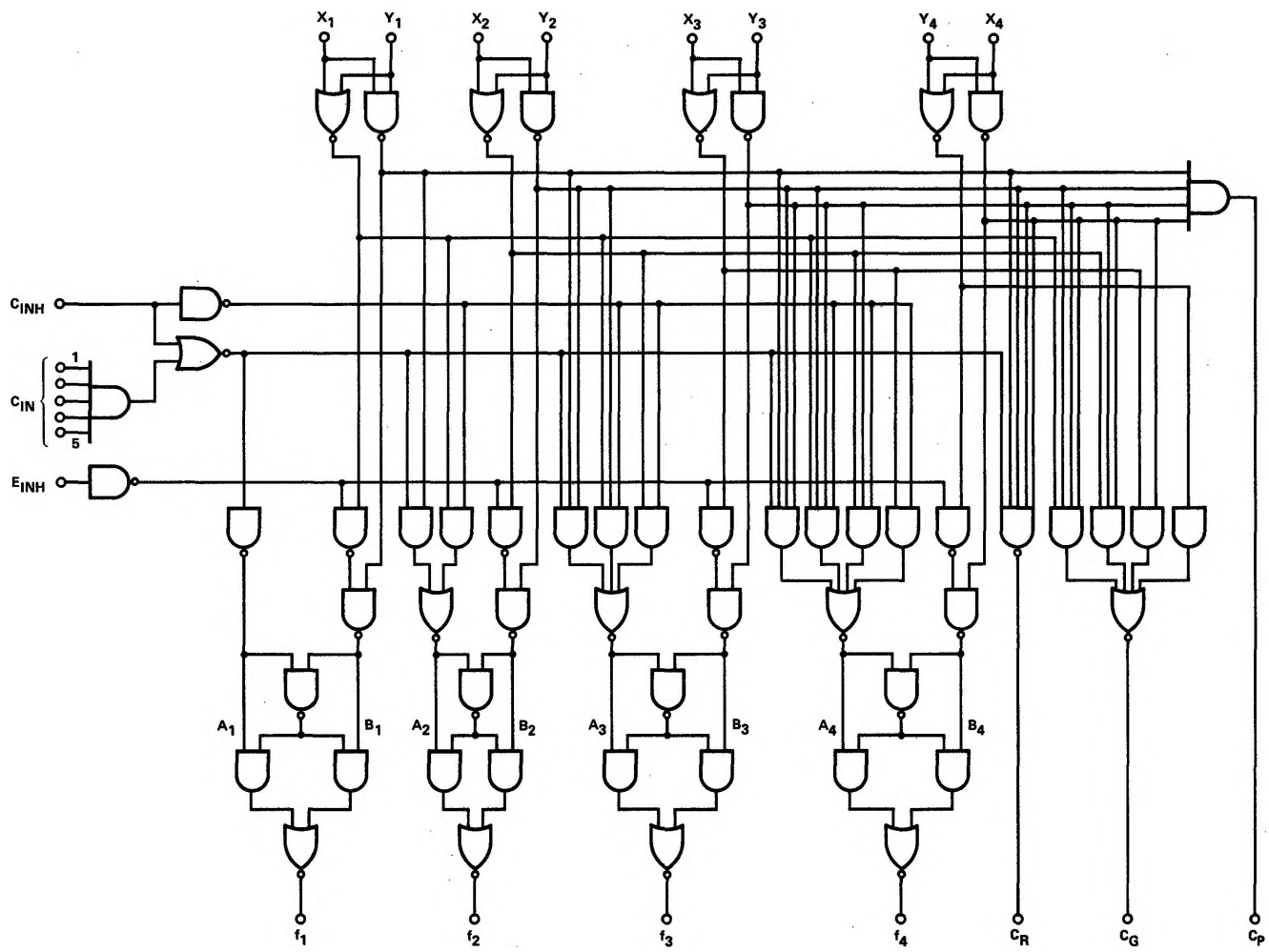
The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder, the 8260 permits high speed parallel addition of four sets of data and features both simultaneous addition on a character to character and on a bit to bit basis within the package.

When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G); Propagated (C_p); and Ripple (C_R). This gives the 8260 complete flexibility when used in Ripple Carry or Anticipated Carry Adder Systems.

LOGIC DIAGRAM



A and B refer to functional block diagram on Page 76

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUT TERMINALS					OUTPUT TERMINALS (mA)				NOTES
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
"1" Output Voltage	2.6	3.5		V	2.0	2.0	2.0	2.0	2.0		-0.8	-0.8	-0.8	1
"0" Output Voltage														
f_n, C_G and C_R			0.4	V	0.8	0.8	0.8	0.8	0.8		9.6	9.6	9.6	2
"0" Input Current														
X_n and C_{INH}	-0.1		-3.2	mA	0.4	5.25		0.4						
Y_n	-0.1		-3.2	mA	5.25	0.4								
E_{INH} & C_{IN1}, through C_{IN5}	-0.1		-1.6	mA			0.4		0.4					3
"1" Input Current														
X_n and C_{INH}			80	μA	4.5	0V		4.5						
Y_n			80	μA	0V	4.5								
E_{INH} & C_{IN1}, through C_{IN5}			40	μA			4.5		4.5					4
Input Latch Voltage														
X_n and C_{INH}	5.5			V	10mA	0V		10mA						
Y_n	5.5			V	0V	10mA								
E_{INH} & C_{IN1}, through C_{IN5}	5.5			V			10mA		10mA					4
Power/Current Consumption			400/ 76.2	600/ 114.1	mW/ mA									15

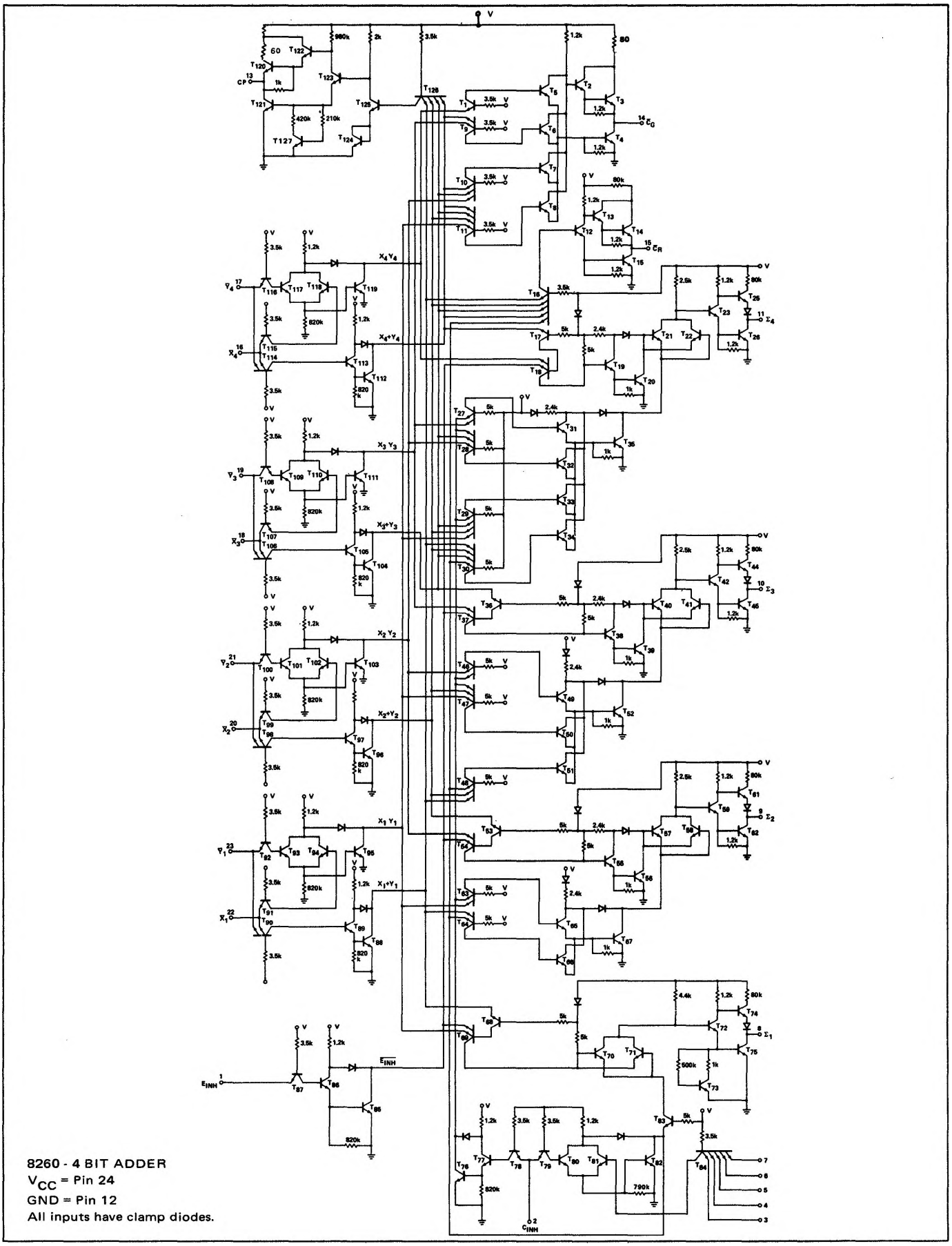
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUT TERMINALS					OUTPUT TERMINALS (mA)				NOTES
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
Propagation Delay														
X_n, Y_n and C_{IN} to C_R		14	20	ns										14
X_n and Y_n to Cp and C_G		14	20	ns										14
X_n and Y_n to f_n		24	33	ns										14
C_{IN} to f_n		14	22	ns										14
Output Short Circuit Current														
f_n, C_G and C_R	-20		-70	mA	5.0	5.0	5.0	5.0	5.0		0V	0V	0V	13
Cp	-40		-90	mA	0V					0V				

NOTES:

1. Output source current is supplied through a resistor to ground.
2. Output sink current is supplied through a resistor to V_{CC}.
3. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to V_{CC}.
4. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to ground.
5. Keep unused inputs tied to V_{CC} unless otherwise specified.
6. All voltage and capacitance measurements are referenced to the ground terminal.
7. All measurements are taken with ground pin tied to "0" volts.
8. Positive current flow is defined as into the terminal referenced.
9. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
10. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. Input latch voltage test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Ground one output at a time.
14. Measure switching times at 1.5 volt level.
15. V_{CC} = 5.25V.

SCHEMATIC DIAGRAM



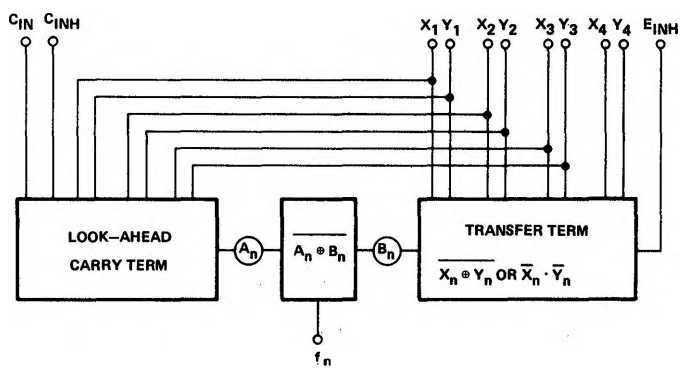
8260 - 4 BIT ADDER
V_{CC} = Pin 24
GND = Pin 12
All inputs have clamp diodes.

MODE OF OPERATION

INPUTS	Least Significant C_{IN} Inputs to be *	CONTROLS C_{INH}	CONTROLS E_{INH}	f	
X_n, Y_n	0	0	0	Σ_n	Add
	0	0	1	--	Not Used
	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$	1	0	0	$\overline{\Sigma}_n$	Add
	1	0	1	---	Not Used
	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

*Least significant of a "Multiple Package" adder system.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

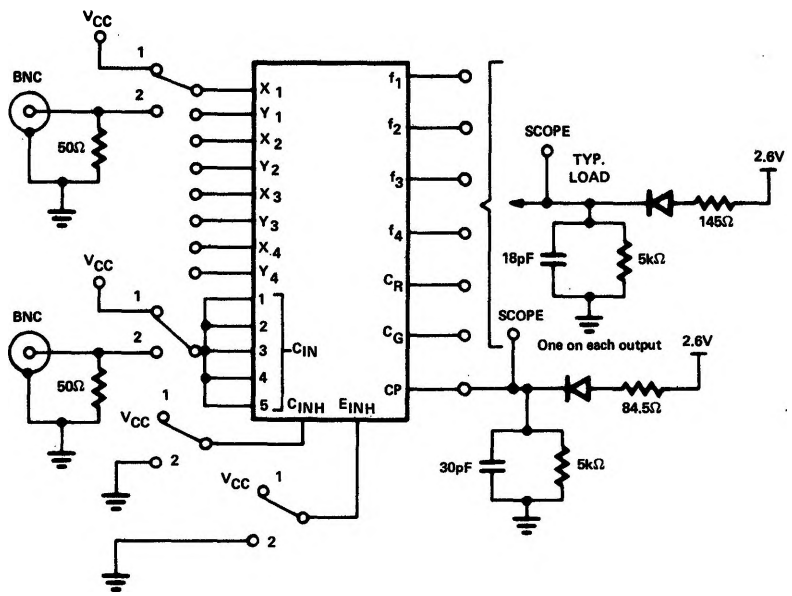
$C_{INH} = 1 \longrightarrow A_n = 1$
$C_{INH} = 0 \longrightarrow A_n = \longrightarrow$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

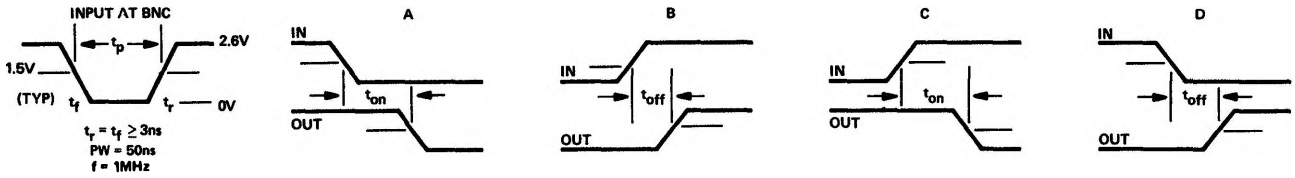
A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

AC TEST FIGURE AND WAVEFORMS



NOTE: Scope terminals to be ≤ ½" from Package Pins.



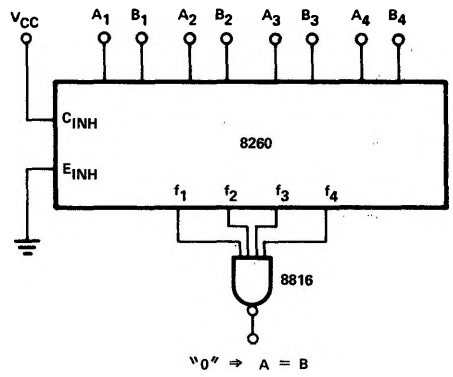
STEP NO.	DELAY FROM-TO	SWITCH POSITION												WAVEFORM TYPE
		DRIVEN INPUTS	OTHER INPUTS											
			X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	C_{IN}	E_{INH}	C_{INH}	
1	X_n to C_R or X_n to C_P	2	2	1	2	1	2	1	2	1	2	2	2	A, B C, D
2	Y_n to C_R or Y_n to C_P	2	1	2	1	2	1	2	1	2	2	2	2	A, B C, D
3	X_n,Y_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	A, B
4	C_{IN} to C_R	2	2	2	2	2	2	2	2	2	2	2	2	A, B
5	C_{IN} to f_n	2	1	2	1	2	1	2	1	2	2	2	2	C, D

TYPICAL APPLICATIONS

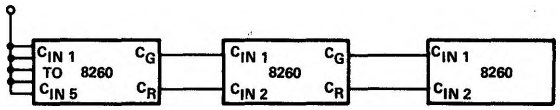
The 8260 contains the control logic necessary to allow operation as a general purpose arithmetic logic device. Below, the internal carries are inhibited to effect Exclusive-NOR or coincidence operation. The 8260 may also be operated as four independent AND gates to implement masking and similar requirements of micro-programming.

The Ripple Adder System is the simplest but also the slowest application of the 8260. The typical total addition time (input to sum output for 12-bit ripple adder is 42ns.).

FOUR-BIT COMPARATOR

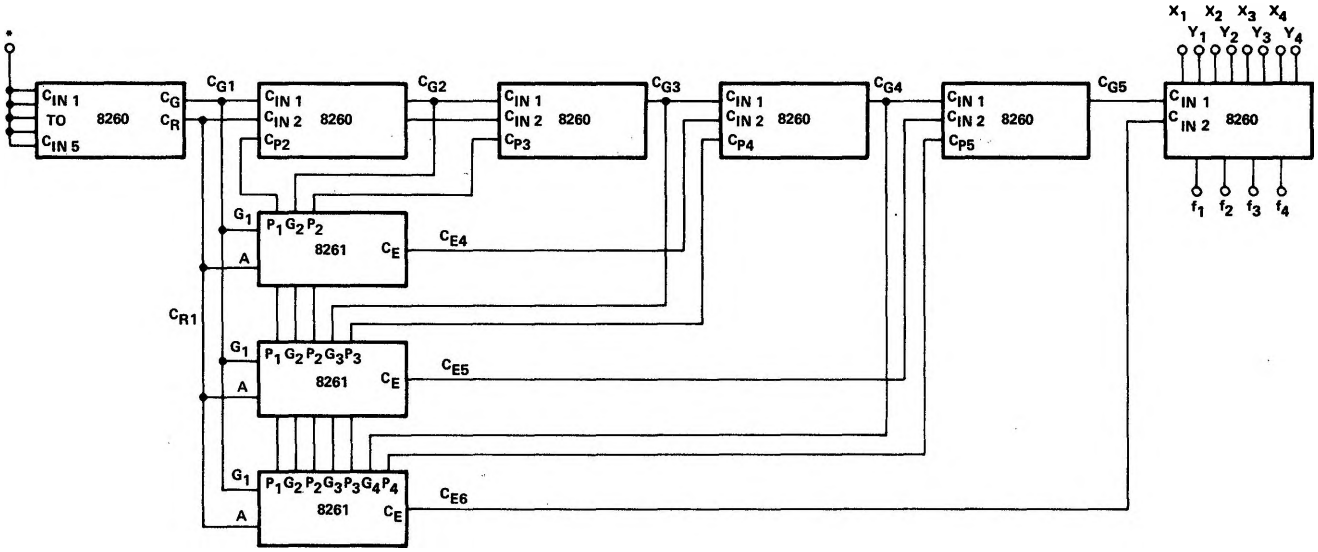


RIPPLE ADDER SYSTEM



The Fast Adder System provides complete carry look-ahead addition for words to 24 bits in length and is the fastest application of the 8260 units. The typical total addition time for a 24 bit fast adder is 42ns.

24-BIT FAST ADDER SYSTEM



*Tied to V_{CC} if Not-True Inputs Are Used, Otherwise to Ground.