3-INPUT, 4-BIT DIGITAL MULTIPLEXER

REFER TO PAGE 15 FOR P, N AND Y PACKAGE PIN CONFIGURATIONS.
8263
8264

## DIGITAL 8000 SERIES TTL/MSI

## DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.
The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus,
eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.
TRUTH TABLE

| Data Input $A_{n} B_{n} C_{n}$ | $\begin{aligned} & \hline \text { Channel } \\ & \text { Select } \\ & \mathrm{S}_{0} \mathrm{~S}_{1} \\ & \hline \end{aligned}$ | Data Complement | Output Enable (8264) | Data Outputs |
| :---: | :---: | :---: | :---: | :---: |
| $A_{n} \times \times$ | 11 | 0 | 1 | $A_{n}$ |
| $x B_{n} \times$ | 01 | 0 | 1 | $B_{n}$ |
| $x \times C_{n}$ | 10 | 0 | 1 | $\mathrm{C}_{n}$ |
| $\times \times \times$ | 00 | 0 | 1 | 0 |
| $A_{n} \times \times$ | 11 | 1 | 1 | $\bar{A}_{n}$ |
| $x B_{n} \times$ | 01 | 1 | 1 | $\bar{B}_{n}$ |
| $\times \times C_{n}$ | 10 | 1 | 1 | $\bar{C}_{n}$ |
| $\times \times \times$ | 00 | 1 | 1 | 1 |
| $\mathrm{x} \times \mathrm{x}$ | $\times \mathrm{x}$ | x | 0 | 1 |

$X=$ Either State

## LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | $A_{n}$ | $B_{n}$ | $C_{n}$ | $S_{0}$ | $S_{1}$ | DATA COMP | OUTPUT ENABLE | OUTPUTS |  |
| "1" Output Voltage (8263) | 2.6 | 3.5 |  | V | 2.0 V | 2.0V | 2.0V | 2.0 V | 2.0 V | 0.8 V |  | $800 \mu \mathrm{~A}$ | 8 |
| "1" Output Leakage Current (8264) |  |  | 200 | $\mu \mathrm{A}$ | 2.0 V | 2.0V | 2.0 V | 2.0 V | 2.0 V | 0.8 V | 2.0 V |  | 11 |
| "0" Output Voltage (8263) |  |  | 0.4 | V | 0.8 V | 0.8V | 0.8V | 2.0 V | 2.0 V | 0.8V |  | 9.6 mA | 9 |
| "00" Output Voltage (8264) |  |  | 0.4 | V | 0.8V |  |  |  |  |  |  | 16.0 mA | 11 |
| "0" Input Current |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $A_{n}$ | -0.1 |  | -1.6 | mA | 0.4V |  |  |  |  |  |  |  |  |
| $B_{n}$ | -0.1 |  | -1.6 | mA |  | 0.4V |  | 0.4V |  |  |  |  |  |
| $C_{n}$ | -0.1 |  | -1.6 | mA |  |  | 0.4V |  | 0.4 V |  |  |  |  |
| OE, DC | -0.1 |  | -1.6 | mA |  |  |  |  |  | 0.4 V | 0.4 V |  | 6 |
| $\mathrm{S}_{0}, \mathrm{~S}_{1}$ | -0.1 |  | -3.2 | mA |  |  |  | 0.4V | 0.4V |  |  |  |  |
| "1" Input Current |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $A_{n}$ |  |  | 40 | $\mu \mathrm{A}$ | 4.5 V |  |  | OV | OV |  |  |  |  |
| $B_{n}$ |  |  | 40 | $\mu \mathrm{A}$ |  | 4.5V |  |  | OV |  |  |  |  |
| $C_{n}$ |  |  | 40 | $\mu \mathrm{A}$ |  |  | 4.5V | OV |  |  |  |  |  |
| OE, DC |  |  | 40 | $\mu \mathrm{A}$ |  |  |  |  |  | 4.5 V | 4.5 V |  |  |
| $\mathrm{S}_{0} \cdot \mathrm{~S}_{1}$ |  |  | 40 | $\mu \mathrm{A}$ |  |  |  | 4.5 V | 4.5V |  |  |  |  |

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$


NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
"UP" Level $=" 1 "$ " "DOWN" Level $=" 0 "$.
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electric Corporation

Model 75A-S8 Capacitance Bridge or equivalent. f=1 MHz, $V_{\text {ac }}=25 \mathrm{~m}$ Vrms. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$. 10. Refer to AC Test Figure.
11. Connect an external $1 k \pm 1 \%$ resistor from $V_{C C}$ to the output for this test.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. $\quad V_{C C}=5.25$ volts.

SCHEMATIC DIAGRAMS



AC TESTING

| Step No. | Delay From-To | Switching Positions |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Waveform Types |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Driven Inputs | Other Inputs |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | $A_{0}$ | $\mathrm{B}_{0}$ | $\mathrm{C}_{0}$ | A1 | $\mathrm{B}_{1}$ | $\mathrm{C}_{1}$ | A2 | B2 | $\mathrm{C}_{2}$ | $A_{3}$ | $\mathrm{B}_{3}$ | $\mathrm{C}_{3}$ | OE | OE | OE | $\mathrm{S}_{0}$ | $\mathrm{S}_{1}$ | DC |  |
| 1 | $A_{n}$ to $f_{n}$ | 2 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | C, D |
| 2 | $S_{0}$ to $f_{n}$ | 2 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | A, B |
| 3 | $S_{0}$ to $f_{n}$ | 2 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | C, D |
| 4 | $S_{1}$ to $f_{n}$ | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | C, D |
| 5 | $D C$ to $f_{n}$ | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | C, D |
| 6 | $O E_{n}$ to $f_{n}$ | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | 1 | 1 | 1 | C, D |

NOTE: Step number 6 is for 8264 only.
*Test one input at a time - others remain at " 1 ".
AC TEST FIGURE AND WAVEFORMS


## NON-INVERTING PATHS

Amplitude $=2.6 \mathrm{~V}$
PW = 200ns
$P R R=1 \mathrm{MHz}$

$t_{r}=t_{f} \leqslant 3 n s$


INVERTING PATHS


## TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to select a particular 8264. All non-selected 8264's have their outputs in the logic " 1 " condition, thus allowing the selected multiplexer to predominate.

EXPANDING THE 8264


Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3 -register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263 . Now there are three different presettable 4 -bit words that can be chosen by the 8264 . By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

## VARIABLE MODULUS COUNTER



