DESCRIPTION

The 82S16 and 82S17 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and −250μA (S82S16/17) or −100μA (N82S16/17) for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S16 and 82S17 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S16/17, B or F. For the military temperature range (−55°C to +125°C) specify S82S16/17, F only.

FEATURES

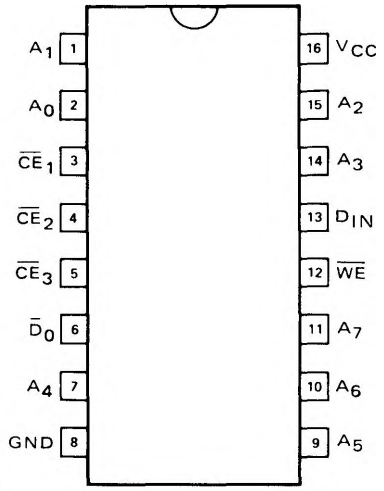
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 55ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
  S82S16, S82S17 – (−250μA) MAXIMUM
  N82S16, N82S17 – (−100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- 16 PIN CERAMIC DIP
- OUTPUT OPTION:
  TRI-STATE – 82S16
  OPEN COLLECTOR – 82S17

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



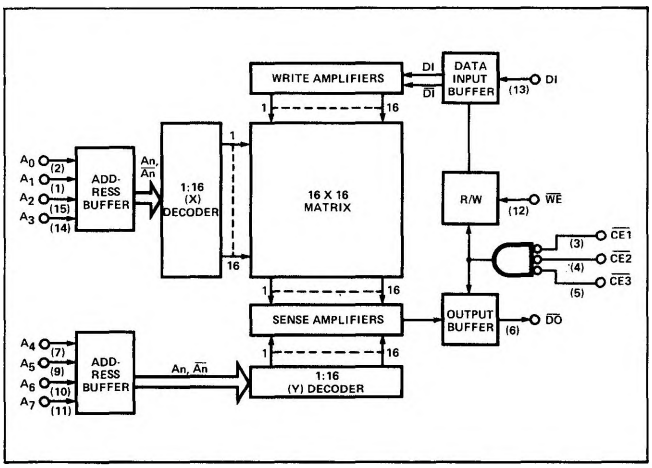
*B – Plastic
C – Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16	82S17
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S17)	+5.5	Vdc
V_O	Off-State Output Voltage (82S16)	+5.5	Vdc
T_A	Operating Temperature Range		
	S82S16/17	−55° to +125°	°C
	N82S16/17	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		N82S16/17			S82S16/17			UNIT	NOTES
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = MAX		2.0			2.0			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = MIN				0.85			0.8	V	
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA			−1.0	−1.5		−1.0	−1.5	V	1, 8
V_{OH}	High-Level Output Voltage (82S16)	V_{CC} = MIN, I_{OH} = −3.2mA		2.6			2.4			V	1, 6
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA			0.35	0.45		0.35	0.5	V	1, 7
I_{OLK}	Output Leakage Current (82S17)	V_{OUT} = 5.5V			1	40		1	40	μA	5
$I_{O(OFF)}$	Hi-Z State Output Current (82S16)	V_{OUT} = 5.5V			1	40		1	50	μA	5
		V_{OUT} = 0.45V			−1	−40		−1	−50	μA	5
I_{IH}	High-Level Input Current	V_{CC} = MAX, V_{IN} = 5.5V			1	25		1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = MAX, V_{IN} = 0.45V			−10	−100		−10	−250	μA	8
I_{OS}	Short-Circuit Output Current (82S16)	V_{CC} = MAX, V_O = 0V		−20		−70	−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX			80	115		80	120	mA	4
	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX, T_A = +125°C							99	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5			5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	V_{CC} = 5.0V		8			8		pF	

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

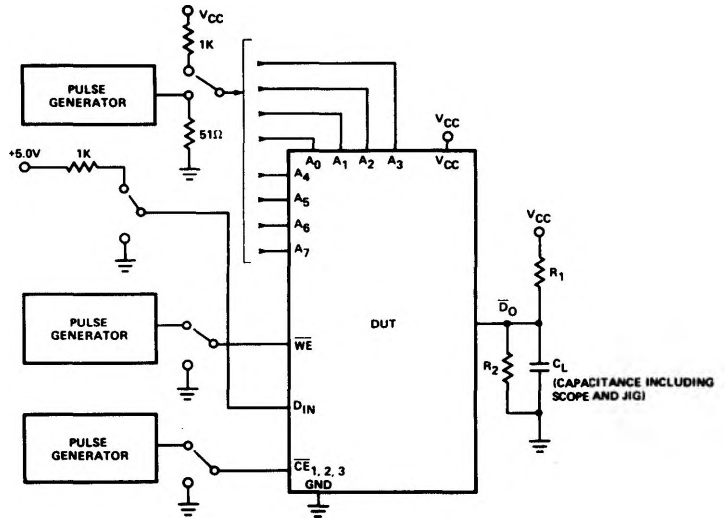
SWITCHING CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

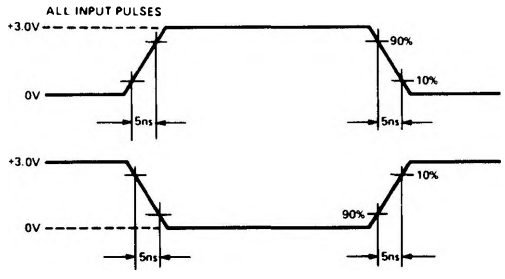
PARAMETER		TEST CONDITIONS	S82S16/17			N82S16/17			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delay									
T_{AA}	Address Access Time	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$		40	70		40	50	ns
T_{CE}	Chip Enable Access Time			30	40		30	40	ns
T_{CD}	Chip Enable Output Disable Time			30	40		30	40	ns
T_{WD}	Write Enable to Output Valid Time			30	55		30	40	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	20	5		20	5		ns
T_{WSD}	Data In to Write Enable		50	40		40	30		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		10	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width	Note 2	40	20		30	15		ns

AC TEST LOAD

LOADING CONDITION



INPUT PULSES

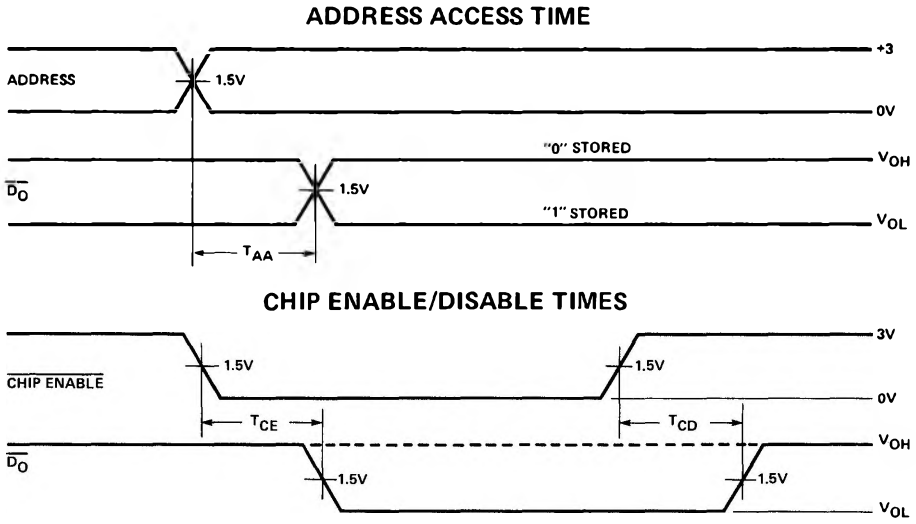


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

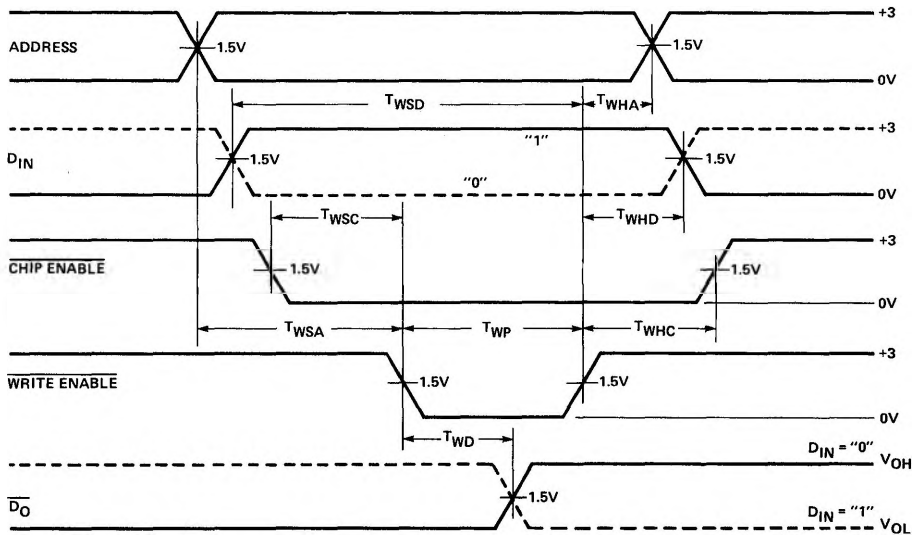
NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
T_{CD}	Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
T_{AA}	Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
T_{WSC}	Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.
T_{WHD}	Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.
T_{WP}	Width of WRITE ENABLE pulse.
T_{WSA}	Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
T_{WSD}	Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
T_{WD}	Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.
T_{WHC}	Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
T_{WHA}	Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.