SIGNETICS DCL INTEGRATED CIRCUITS

8826 DUAL J-K BINARY

The 8826 is a capacitively coupled, high-speed, Dual J-K Binary intended for use in systems requiring storage and counting rates up to 25MHz. Two completely separate binaries are provided with common connections only at V_{CC} and ground. Separate J, K, Clock, Q and $\overline{Q}$, and Reset lines are provided for each binary. The AC clock steering network provides high speed operation with low power consumption.

This element responds to the trailing or negative-going transition of the clock pulse. The Reset line may be activated regardless of the state of the clock.

Characterization of each logic element in the 8800 group includes loading rules for driving the 8826. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Detailed usage and applications information may be found in Section 4.

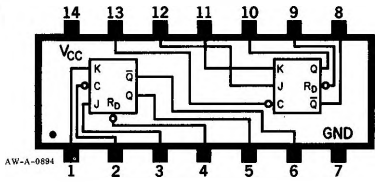
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8826	TEMP. N8826	Vcc	RESET	CLOCK	J	K	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V				-250μA	8, 12
A-3	Q_1, Q_2	2.8			V	+25°C	+25°C	5.0V	2.0V				-250μA	8, 12
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V				-250μA	8, 12
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V				-250μA	8
A-3	$\overline{Q}_1, \overline{Q}_2$	2.8			V	+25°C	+25°C	5.0V	0.8V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.7V				-250μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	0.8V				8.0mA	9
A-3	Q_1, Q_2			0.40	V	+25°C	+25°C	5.0V	0.8V				8.0mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	0.7V				8.0mA	9
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V				8.0mA	9, 12
A-3	$\overline{Q}_1, \overline{Q}_2$			0.40	V	+25°C	+25°C	5.0V	2.0V				8.0mA	9, 12
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V				8.0mA	9, 12
C-1	"0" INPUT CURRENT			-2.4	mA	-55°C	0°C	5.25V			0.40V	0.40V		
A-3	J_1, K_1, J_2, K_2			-2.4	mA	+25°C	+25°C	5.25V			0.40V	0.40V		
C-1				-2.4	mA	+125°C	+75°C	5.25V			0.40V	0.40V		
C-1	"0" INPUT CURRENT			-2.0	mA	-55°C	0°C	5.25V	0.40V					
A-3	$RESET_1, RESET_2$			-2.0	mA	+25°C	+25°C	5.25V	0.40V					
C-1				-2.0	mA	+125°C	+75°C	5.25V	0.40V					
C-1	"0" INPUT CURRENT			-10	μA	+25°C	+25°C	5.25V		0.40V				
A-3	CP_1, CP_2 (CLOCK)			-10	μA	+25°C	+25°C	5.25V		0.40V				
C-1				-10	μA	+125°C	+75°C	5.25V		0.40V				
A-4	"1" INPUT CURRENT $J_1, J_2, K_1, K_2, RESET_1, RESET_2$			25	μA	+125°C	+75°C	5.0V	4.5V		4.5V	4.5V		13
A-4	"1" INPUT CURRENT CP_1, CP_2, (CLOCK)			25	μA	+125°C	+75°C	5.0V		4.5V				
A-2	POWER CONSUMPTION (Per Binary)			64	mW	+25°C	+25°C	5.25V						
A-2	OUTPUT SHORT CIRCUIT CURRENT $\overline{Q}_1, \overline{Q}_2$ ONLY	-20		-70	mA	+25°C	+25°C	5.0V	0V				0V	
C-1	INPUT LATCH VOLTAGE $J_1, J_2, K_1, K_2, RESET_1, RESET_2$	6.5			V	+25°C	+25°C	5.0V	10mA		10mA	10mA		13, 14
	CP_1, CP_2	5.0		6.0	V	+25°C	+25°C	5.0V		10μA				
A-6	TURN-ON DELAY			35	ns	+25°C	+25°C	5.0V					D.C. F.O.-10	10, 16
A-6	TURN-OFF DELAY			20	ns	+25°C	+25°C	5.0V					D.C. F.O.-10	10, 16
A-6	TOGGLE RATE	25			MHz	+25°C	+25°C	5.0V						16
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V					A.C. F.O. 2	11, 16
C-2	INPUT CAPACITANCE $J_1, J_2, K_1, K_2, RESET_1, RESET_2$			3.0	pf	+25°C	+25°C	5.0V	2.0V		2.0V	2.0V		7
C-2	INPUT CAPACITANCE CP_1, CP_2, (CLOCK)			50	pf	+25°C	+25°C							7
A-6	CLOCK MODE HOLDING TEST			10	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	CLOCK MODE SWITCHING TEST			50	ns	+25°C	+25°C	5.0V		PULSE				16

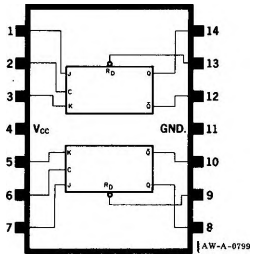
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA
11. One AC fan-out is defined as 50pf.
12. Momentarily apply zero volts to $\overline{Q}$ and V_{CC} to Q to ensure state of the binary element prior to test measurement.
13. To test "1" INPUT CURRENT AND LATCH VOLTAGE RATING for J and RESET, ensure Q = "0". To test "1" INPUT CURRENT AND LATCH VOLTAGE RATING for K, ensure $\overline{Q}$ = "0".
14. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



J PACKAGE



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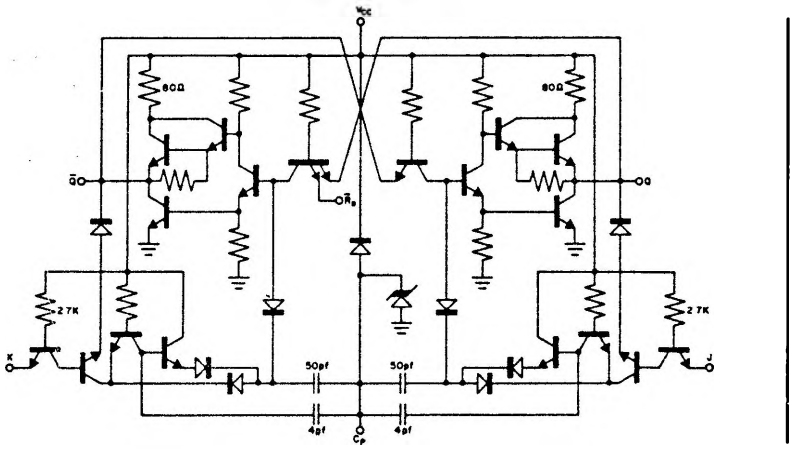
BASIC CIRCUIT SCHEMATIC



TRUTH TABLE

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

$\bar{R}_D = 0 \Rightarrow Q = 0$

n is time prior to clock
n+1 is time following clock