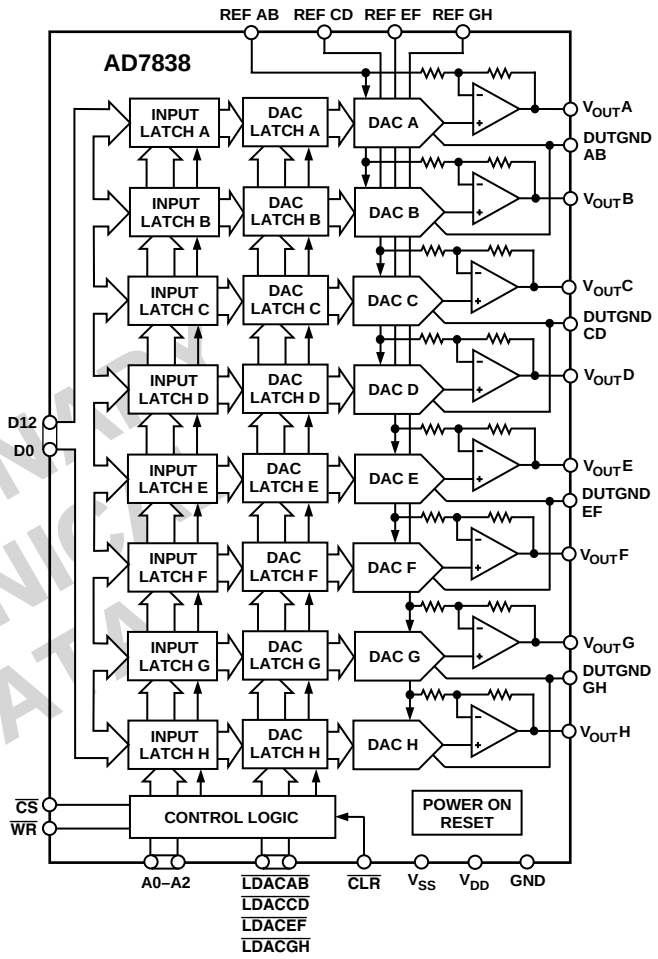
Octal, 13-Bit Voltage-Output DAC with Parallel Interface

AD7838

FEATURES
Eight 13-Bit DACs in One Package
Full 13-Bit Performance without Adjustments
Buffered Voltage Outputs
Offset Adjust for Each DAC Pair
±5 V Supply Operation
Unipolar or Bipolar Output Swing to ±4.5 V
Output Settling to 1/2 LSB in 5 μs
Double Buffered Digital Inputs
Microprocessor and TTL/CMOS Compatible
Asynchronous Load Facility using $\overline{\text{LDAC}}$ Inputs
Clear Function to User-Defined Voltage
Power-On-Reset, Outputs Power Up at DUTGND
44-Lead PLCC Package
Pin Compatible with MAX547

APPLICATIONS
Process Control
Automatic Test Equipment
General Purpose Instrumentation
Digital Offset and Gain Adjustment
Arbitrary Function Generators
Avionics Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7838 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). The output voltages are provided through on-chip precision output amplifiers into which an external offset voltage can be inserted via the DUTGND pins. The AD7838 operates from a ±5 V ± 5% supply. Bipolar output voltages with up to ±4.5 V voltage swing can be achieved with no external components. The AD7838 has four separate reference inputs; each is connected to two DACs, providing different scale output voltages for every DAC pair.

The AD7838 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous $\overline{\text{LDAC}}$ input transfers data from the input latch to the DAC latch. The four $\overline{\text{LDAC}}$ inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all $\overline{\text{LDAC}}$ pins. An asynchronous clear input resets the output of all eight DACs to the relevant DUTGND. Asserting $\overline{\text{CLR}}$ resets both the DAC and the input latch to bipolar zero (1000 Hex). On power-up, reset circuitry performs the same function as $\overline{\text{CLR}}$. All logic inputs are TTL/CMOS compatible.

The AD7838 is available in a 44-lead PLCC package.

REV. 0

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AD7838–SPECIFICATIONS

(V_{DD} = +5 V; V_{SS} = –5 V; DUTGNDXX = GND = 0 V; R_L =10 kΩ and C_L = 50 pF to GND, T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	B	Units	Test Conditions/Comments
ACCURACY			
Resolution	13	Bits	
Relative Accuracy	±2	LSB max	Typically ±0.5 LSB
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic Over Temperature
Bipolar Zero-Code Error	±20	LSB max	Typically ±5 LSB
Gain Error	±8	LSB max	Typically ±1 LSB
V_{DD} Power Supply Rejection[2]	±0.0025	%/% max	$\Delta Gain/\Delta V_{DD}$
V_{SS} Power Supply Rejection[2]	±0.0025	%/% max	$\Delta Gain/\Delta V_{SS}$
Load Regulation	0.3	LSB typ	R_L = Unloaded to 10 kΩ
REFERENCE INPUTS[3, 4]			
Input Range	DUTGND	V min	
	V_{DD}	V max	
Input Impedance	5	kΩ min	
OUTPUT CHARACTERISTICS			
Maximum Output Voltage	V_{DD} – 0.5	V max	
Minimum Output Voltage	V_{SS} + 0.5	V min	
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate	3	V/µs typ	
Output Settling Time	5	µs typ	Settling to 0.5 LSB of Full Scale[5]
Digital Feedthrough	5	nV-s typ	
Digital Crosstalk	5	nV-s typ	
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	V_{IN} = 0 V or V_{DD}
C_{IN}, Input Capacitance[6]	10	pF max	
POWER REQUIREMENTS			
V_{DD}	5	V nom	±5% for Specified Performance
V_{SS}	–5	V nom	±5% for Specified Performance
I_{DD}	44	mA max	Typically 14 mA
I_{SS}	40	mA max	Typically 11 mA

NOTES

[1]Temperature Range for B Version: –40°C to +85°C.

[2]PSRR is tested by changing the respective supply voltage by ±5%.

[3]For best performance, REFxx should be greater than DUTGNDxx by 2 V and less than V_{DD} – 0.6 V. The device operates with reference inputs outside this range, but performance may degrade.

[4]Reference input resistance is code dependent.

[5]Typical settling time with 1000 pF capacitive load is 10 µs.

[6]Guaranteed by design, not production tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5 V; V_{SS} = –5 V; DUTGND = GND = 0 V, REFxx = 4.096 V)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	10	ns min	Address Valid to $\overline{WR}$ Setup Time
t_2	0	ns min	Address Valid to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulse Width
t_4	50	ns min	$\overline{WR}$ Pulse Width
t_5	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_6	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_7	50	ns min	Data Valid to $\overline{WR}$ Setup Time
t_8	0	ns min	Data Valid to $\overline{WR}$ Hold Time
t_9	5	µs typ	Output Settling Time
t_{10}	100	ns min	$\overline{CLR}$ Pulse Width
t_{11}	50	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. Timing applies for all grades of the part.
[2]Rise and fall times should be no longer than 50 ns.

Specifications subject to change without notice.

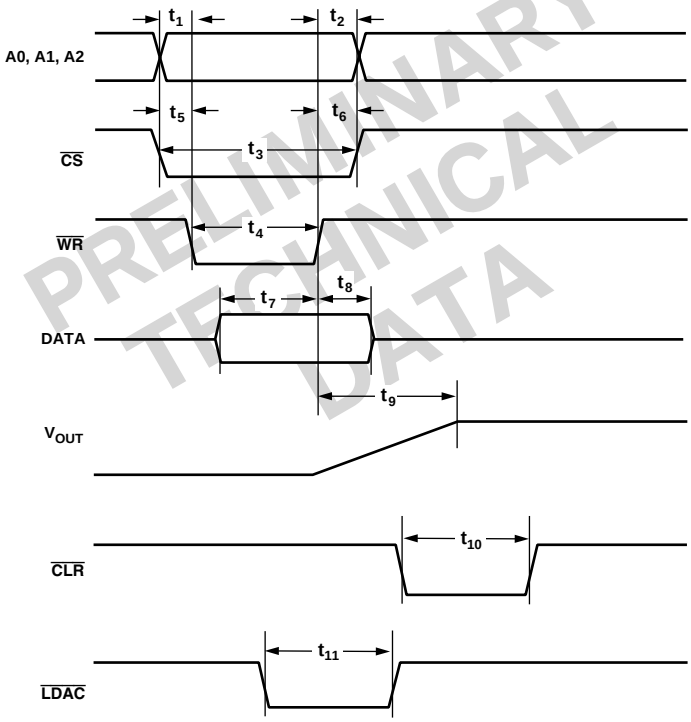


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

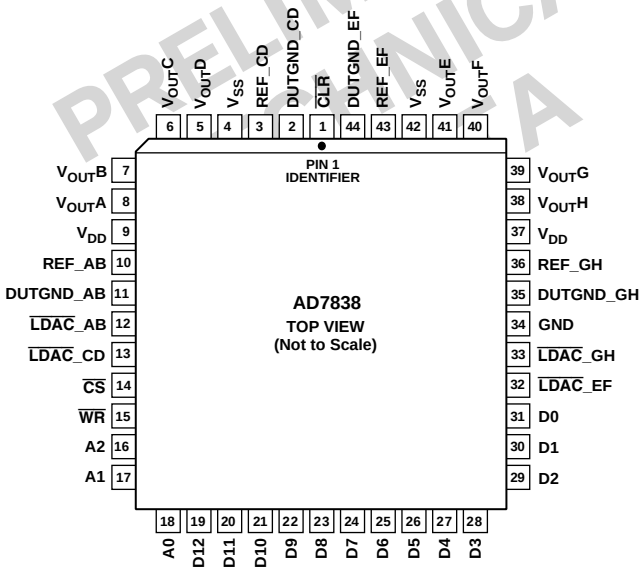
V_{DD} to GND ..... –0.3 V to +6 V
V_{SS} to GND ..... +0.3 V to –6 V
Digital Inputs to GND ..... –0.3 V to V_{DD} +0.3 V
REFxx ..... DUTGND – 0.3 to V_{DD} +0.3
DUTGNDxx ..... V_{SS} – 0.3 to V_{DD} +0.3
V_{OUT} ..... V_{DD} to V_{SS}
Max Current Into REFxx Pin ..... ±10 mA
Max Current Into Any Other Signal Pin ..... ±50 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
PLCC Package, Power Dissipation ..... TBD mW
θ_{JA} Thermal Impedance ..... 48°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latchup.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy (LSBs)	DNL (LSBs)	Package Description	Package Option
AD7838BP	–40°C to +85°C	±2	±1	Plastic Leaded Chip Carrier (PLCC)	P-44A

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7838 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.