+2.5 V to +5.5 V, 25 MHz Low Power CMOS Complete DDS

Preliminary Technical Information AD9833

FEATURES
+2.5 V to +5.5 V Power Supply
25 MHz Speed
Serial Loading
Sinusoidal/Triangular DAC Output
Power-Down Option
Narrowband SFDR > 72 dB
20 mW Power Consumption at 3 V
10-Pin mSOIC

APPLICATIONS
Digital Modulation
Portable Equipment
Test Equipment
DDS Tuning

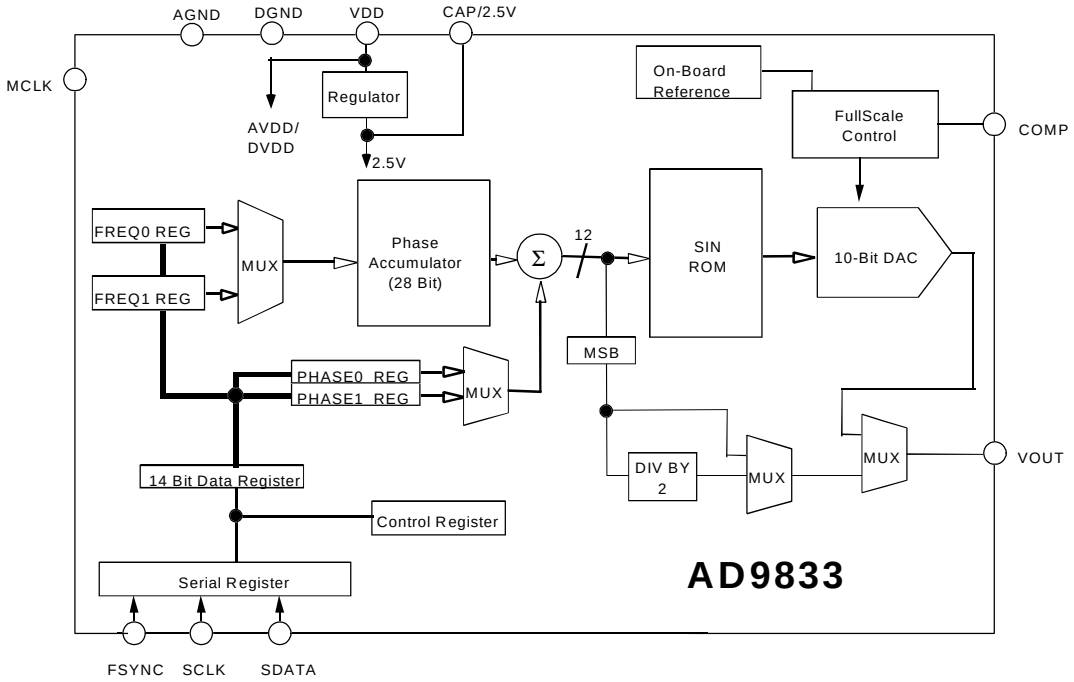
GENERAL DESCRIPTION

This low power DDS device is a numerically controlled oscillator employing a phase accumulator, a sine look-up table and a D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 25 MHz are supported with a power supply from +2.5 V to +5.5 V. Frequency accuracy can be controlled to one part in 0.25 billion. Modulation is effected by loading registers through the serial interface. The digital section is internally operated at +2.5 V, irrespective of the value of VDD, by an on board regulator which steps down VDD to +2.5 V. The ROM can be bypassed so that a linear up/down ramp is output from the DAC. Also, if a clock output is required, the signal data bit can be output.

A power-down pin allows external control of a power-down mode. In addition, sections of the device which are not being used can be powered down to minimise the current consumption. For example, the DAC can be powered down when the MSB is required. The part is available in a 10-pin mSOIC package.

FUNCTIONAL BLOCK DIAGRAM



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SPECIFICATIONS[1]

(V_{DD} = +2.5 V to +5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; R_{SET} = 3.9 kΩ; R_{LOAD} = 200Ω for VOUT unless otherwise noted)

Parameter	AD9833B	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	25	MSPS max	
I_{OUT} Full Scale	3	mA max	
Output Compliance	1	V max	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS			
Dynamic Specifications			
Signal to Noise Ratio	50	dB min	f_{MCLK} = f_{MAX}, f_{OUT} = 1.5 kHz
Total Harmonic Distortion	-53	dBc max	f_{MCLK} = f_{MAX}, f_{OUT} = 1.5 kHz
Spurious Free Dynamic Range (SFDR)			
Wideband (± 2 MHz)	50	dBc min	f_{MCLK} = f_{MAX}, f_{OUT} = f_{MCLK}/3
	55	dBc min	f_{MCLK} = f_{MAX}, f_{OUT} = 0.5 MHz
NarrowBand (± 50 kHz)	72	dBc min	f_{MCLK} = f_{MAX}, f_{OUT} = f_{MCLK}/3
	75	dBc min	f_{MCLK} = f_{MAX}, f_{OUT} = 0.5 MHz
Clock Feedthrough	–55	dBc typ	
Wake Up Time	1	ms typ	
Power-Down Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ +25°C	1.23	Volts typ	
T_{MIN} to T_{MAX}	1.23 ± 7%	Volts min/max	
REFIN Input Impedance	10	MΩ typ	
Reference TC	100	ppm/°C typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	+3.6 V to +5.5 V Power Supply
	VDD - 0.5	V min	+2.7 V to + 3.6 V Power Supply
	2	V min	+2.5 V to +2.7 V Power Supply
V_{INL}, Input Low Voltage	0.9	V max	+3.6 V to +5.5 V Power Supply
	0.5	V max	+2.5 V to + 3.6 V Power Supply
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
POWER SUPPLIES			f_{OUT} = f_{MCLK}/3
AVDD	2.5/5.5	V min/V max	
DVDD	2.5/5.5	V min/V max	
I_{AA}	5	mA max	
I_{DD}	1 + 0.04/MHz	mA typ	
I_{AA} + I_{DD}[2]	7	mA typ	3 V Power Supply
	10	mA max	
	10	mA typ	5 V Power Supply
	15	mA max	
Low Power Sleep Mode	0.25	mA typ	

NOTES

[1]Operating temperature range is as follows: B Version: –40°C to +85°C.

[2]Measured with the digital inputs static and equal to 0 V or DVDD.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +2.5 V to +5.5 V; AGND = DGND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	40	ns min	MCLK Period
t_2	16	ns min	MCLK High Duration
t_3	16	ns min	MCLK Low Duration
t_4	25	ns min	SCLK Period
t_5	10	ns min	SCLK High Duration
t_6	10	ns min	SCLK Low Duration
t_7	5	ns min	$\overline{FSYNC}$ to $\overline{SCLK}$ Falling Edge Setup Time
t_8	10	ns min	FSYNC to SCLK Hold Time
	SCLK - 5	ns max	
t_9	5	ns min	Data Setup Time
t_{10}	3	ns min	Data Hold Time

Guaranteed by design but not production tested.

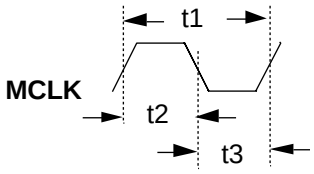


Figure 2. Master Clock

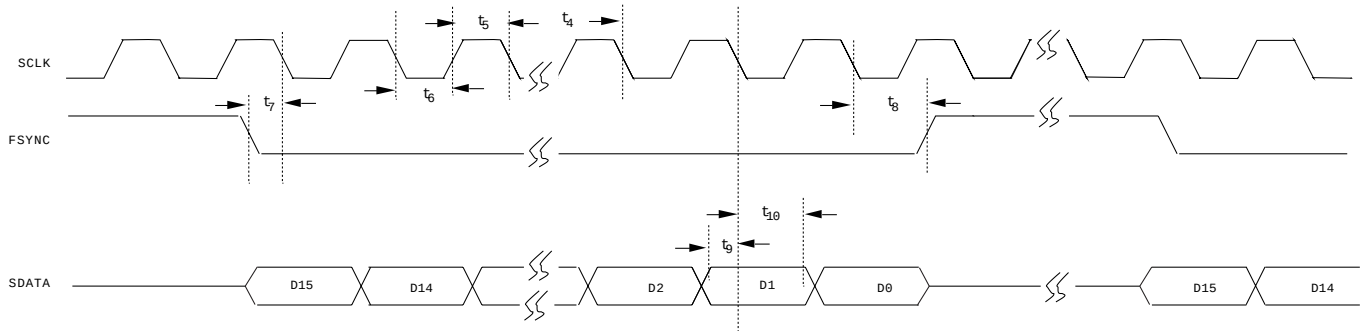


Figure 3. Serial Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AVDD to AGND .....–0.3 V to +7 V
DVDD to DGND .....–0.3 V to +7 V
AVDD to DVDD .....–0.3 V to +0.3 V
AGND to DGND. .....–0.3 V to +0.3 V
Digital I/O Voltage to DGND –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND –0.3 V to AVDD + 0.3 V
Operating Temperature Range
Industrial (B Version) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Maximum Junction Temperature .....+150°C
mSOIC q_{JA} Thermal Impedance .....158°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) .....+215°C
Infrared (15 sec) .....+220°C
ESD Rating ..... > 4500 V

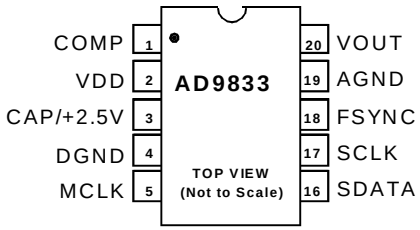
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9833BRM	–40°C to +85°C	10-Pin mSOIC	RM-10

*RM = Micro Small Outline IC (mSOIC).

PIN CONFIGURATION



TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC.

Output Compliance
The output compliance refers to the maximum voltage which can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9833 may not meet the specifications listed in the data sheet.

Spurious Free Dynamic Range
Along with the frequency of interest, harmonics of the fundamental frequency and images of the MCLK frequency are present at the output of a DDS device. The spurious free dynamic range (SFDR) refers to the largest spur or harmonic which is present in the band of interest. The wide band SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the bandwidth
±2 MHz about the fundamental frequency. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±50 kHz about the fundamental frequency.

Clock Feedthrough
There will be feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD9833's output spectrum.

PIN DESCRIPTION

Pin Number	Mnemonic	Function
POWER SUPPLY		
VDD	2	Positive power supply for the analog section and the digital interface sections. The on board 2.5 V regulator is also supplied from VDD. A 0.1 µF and 10 µF decoupling capacitor should be connected between VDD and AGND. VDD can have a value from +2.5 V to +5.5 V.
AGND	9	Analog Ground.
DGND	4	Digital Ground.
CAP/2.5 v	3	The digital circuitry operates from a +2.5 V power supply. This +2.5 V is generated from VDD using an on board regulator. The regulator requires a decoupling capacitor which is connected from CAP/2.5V to DGND. A 1 µF and 0.1 mF capacitor should be connected from CAP/+2.5V to AGND. If the user has a power supply of 2.5V, CAP/2.5V should be tied directly to VDD.
ANALOG SIGNAL AND REFERENCE		
VOUT	10	Voltage Output. An on-chip resistor is connected between VOUT and AGND.
COMP	1	Compensation pin. This is a compensation pin for the internal reference amplifier. A 10 nF typical decoupling ceramic capacitor should be connected between COMP and VDD.
DIGITAL INTERFACE AND CONTROL		
MCLK	5	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
SCLK	7	Serial Clock, Logic Input. Data is clocked into the AD9834 on each falling SCLK edge.
SDATA	6	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
FSYNC	8	Data Synchronisation Signal, Logic Input. When this input is taken low, the internal logic is informed that a new word is being loaded into the device.

Table I. Frequency/Phase Registers

Register	Size	Description
FREQ0 REG	28 Bits	Frequency Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the MCLK frequency.
FREQ1 REG	28 Bits	Frequency Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the MCLK frequency.
PHASE0 REG	12 Bits	Phase Offset Register 0. When PSEL = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1 REG	12 Bits	Phase Offset Register 1. When PSEL = 1, the contents of this register are added to the output of the phase accumulator.

Table 2. Frequency Register Bits

D15	D14	D13		D0
0	1	MSB	14 FREQ0 REG BITS	LSB
1	0	MSB	14 FREQ1 REG BITS	LSB

Table 3. Phase Register Bits

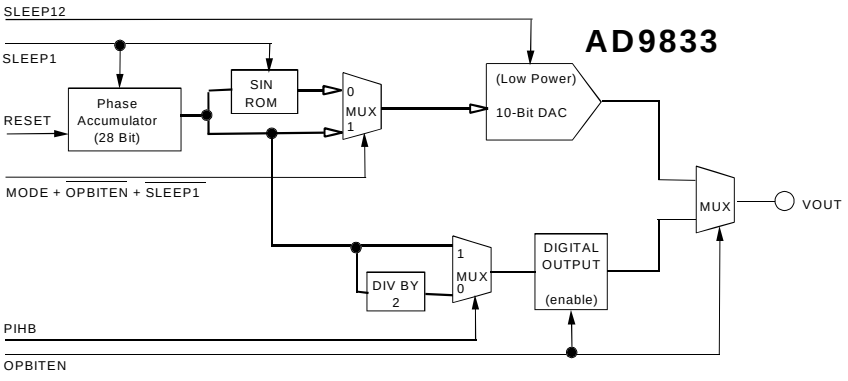
D15	D14	D13	D12	D11		D0
1	1	0	X	MSB	12 PHASE0 REG BITS	LSB
1	1	1	X	MSB	12 PHASE1 REG BITS	LSB

Table 4. Control Register

D15	D14	D13	D0
0	0	CONTROL BITS	

Table 5. Control Register Bits

Bit	Name	Function
D13	B28	Two write operations are required to load a new word into the FREQ registers. When B28 is set to 1, two consecutive writes to the same frequency register are required to load the complete new 28-bit word into that register. The first write to address 01 or 10 contains the 14 LSBs of the frequency word. The next write to this address contains the 14 MSBs. When B28 is set to 0, the frequency register operates as 2 registers, one containing the 14 MSBs and the other containing the 14 LSBs. To alter the 14 MSBs or the 14 LSBs, a single write is made to the FREQ address while D12 of the control register informs the AD9833 whether the bits are MSBs or LSBs.
D12	HLB	When B28 is set to 0, the 14 MSBs of the frequency word can be altered independent of the 14 LSBs and vice versa. A single write is made to the appropriate frequency address while the HLB bit indicates whether the 14 bits being loaded are being transferred to the 14 MSBs or 14 LSBs of the register. This allows the user to continuously load the MSBs or LSBs while ignoring the remaining 14 bits. This is useful if the complete 28 bit resolution is not required. When HLB equals 1, the 14 bits of data are transferred into the 14 MSBs of the frequency register. When HLB equals 0, the 14 LSBs of the frequency register are loaded.
D11	FSELECT	This is the FSELECT bit.
D10	PSEL	This is the PSEL bit.
D9	Reserved	This bit should be set to 0.
D8	RESET	This bit resets the phase accumulator to zero which corresponds to an analog output of midscale. The bit is set to 1 to perform a reset. The accumulator will remain in the reset condition until RESET is set to 0.
D7	SLEEP1	When this bit is set to 1, the internal clock is disabled. The DAC output will remain at its present value as the NCO is no longer accumulating.
D6	SLEEP12	When this bit equals 1, the DAC is powered down. This is useful when the AD9833 is used to output the NCO's MSB only. In this case, the DAC is not required so, it can be powered down to reduce the power consumption.
D5	OPBITEN	When this bit is set to 1, the MSB from the phase accumulator is routed to pin VOUT. It can be sent directly to the pin or, it can be divided by 2 prior to being output. Bit PIHB determines whether the square wave generated by the MSB is divided by 2 before being output. When OPBITEN equals 0, the DAC is connected to VOUT.
D4	Reserved	This bit must be set to 0.
D3	PIHB	This bit is used in association with OPBITEN. When OPBITEN equals 1, the MSB is output on pin VOUT to generate a square wave. When PIHB equals 0, the square wave is divided by 2 before being output. When PIHB equals 1, the MSB is passed directly to the output.
D2	Reserved	This bit must be set to 0.
D1	MODE	When MODE is set to 0 and SLEEP1 and OPBITEN equal 0, the ROM is used to convert the phase information into amplitude information which results in a sinusoidal signal at the output. When MODE is set to 1 and SLEEP1 and OPBITEN equal 0, the ROM is bypassed and the phase information from the phase accumulator is sent directly to the DAC which results in a ramp output.
D0	Reserved	This bit must be set to 0.



DB15 DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADDRS	B28	HLB	FSEL	PSEL	0	RESET	SLEEP1	SLEEP12	OPBITEN	0	PIHB	0	MODE	0