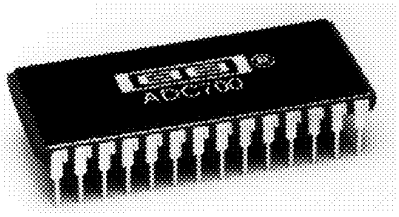
BURR - BROWN®



ADC700

16-Bit Resolution With Microprocessor Interface A/D CONVERTER

FEATURES

- **COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE**
- **CONVERSION TIME: 17µs max**
- **LINEARITY ERROR: ±0.003% FSR max**
- **NO MISSING CODES TO 14 BITS OVER TEMPERATURE**
- **SPECIFIED AT ±12V AND ±15V SUPPLIES**
- **OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY**
- **PARALLEL AND SERIAL DATA OUTPUT**
- **SMALL PACKAGE: 28-Pin DIP**

DESCRIPTION

The ADC700 is a complete 16-bit resolution successive approximation analog-to-digital converter.

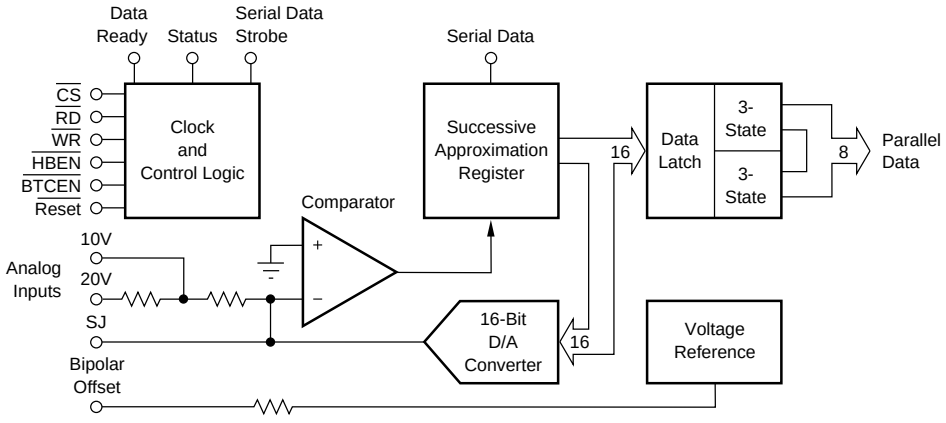
The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V are available.

The conversion time is 17µs max for a 16-bit conversion over the three specification temperature ranges.

After a conversion, output data is stored in a latch separate from the successive approximation logic. This permits reading data during the next conversion, a feature that provides flexible interface timing, especially for interrupt-driven interfaces.

Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700 is available in commercial, industrial and military temperature ranges. It is packaged in a hermetic 28-pin side-braze ceramic DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

© 1989 Burr-Brown Corporation
PDS-856A
Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At T_A = 25°C and at rated supplies: V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V, unless otherwise noted.

	ADC700JH,AH,RH			ADC700KH,BH,SH			
CHARACTERISTICS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels[1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±20			*	µA
Outputs							
Logic Levels							
V_{OL} (I_{OL} = –1.6mA)			+0.4			*	V
V_{OH} (I_{OH} = +20µA)	+2.4			*			V
$I_{LEAKAGE}$							
Data Outputs Only, High Z		10			*		nA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.006			±0.003	% of FSR[2]
Differential Linearity Error			±0.012			±0.006	% of FSR
Gain Error[3]		±0.1	±0.2		*	*	%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Noise at Transitions (3σp-p)		±0.001	±0.003		*	*	% of FSR
Power Supply Sensitivity							
$+V_{CC}$		±0.0015			*		%FSR/%V_{CC}
$-V_{CC}$		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0005			*		%FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8	±15		*	*	ppm/°C
Zero Drift							
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Unipolar Zero		±2	±4		*	*	ppm of FSR/°C
Linearity Drift		±1	±3		*	±2	ppm of FSR/°C
No Missing Codes Temperature Range							
JH (13-bit), KH (14-bit)	0		+70	*		*	°C
AH (13-bit), BH (14 bit)	–25		+85	*		*	°C
RH (13-bit), SH (14-bit)	–55		+125	*		*	°C
CONVERSION TIME 16 bits		15	17		*	*	µs
WARM–UP TIME	5			*			min
OUTPUT DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
$+V_{CC}$	+11.4	+15	+16	*	*	*	VDC
$-V_{CC}$	–11.4	–15	–16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[5]							
$+V_{CC}$		+10	+15		*	*	mA
$-V_{CC}$		–28	–35		*	*	mA
V_{DD}		+17	+20		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	–25		+85	*		*	°C
R, S Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

TIMING SPECIFICATIONS[6]

At V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V, unless otherwise noted.

PARAMETER	LIMIT AT T_A = 25°C	LIMIT AT T_A = 0, +70°C –25°C, +85°C	LIMIT AT T_A = –55°C, +125°C	UNITS	DESCRIPTION
CONVERSION AND SERIAL DATA OUTPUT TIMING					
t_1	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Setup time
t_2	110	130	145	ns, max	$\overline{WR}$ to Status delay
t_3	40	40	40	ns, min	$\overline{WR}$ pulse width
t_4	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_5	15	17	17	µs, max	Conversion time
t_6	550	600	650	ns, max	Data Ready to Status time
t_7	1100	1150	1250	ns, max	$\overline{WR}$ to first Serial Data Strobe
t_8	250	210	200	ns, min	First Serial Data to first Serial Data Strobe
t_9	310	360	400	ns, max	Last Serial Data Strobe to Status
t_{10}	0	0	0	ns, min	Status to $\overline{WR}$ Setup time
PARALLEL DATA OUTPUT TIMING					
t_{11}	0	0	0	ns, min	$\overline{HBEN}$ to $\overline{RD}$ Setup time
t_{12}	0	0	0	ns, min	$\overline{CS}$ to $\overline{RD}$ Setup time
t_{13}[7]	50	58	66	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 20pF (High Byte bus access time)
	70	81	95	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 100pF (High Byte bus access time)
t_{14}	40	40	40	ns, min	$\overline{RD}$ pulse width
t_{15}	40	45	50	ns, max	Data Ready delay from $\overline{RD}$ ($\overline{HBEN}$ asserted)
t_{16}[8]	50	60	65	ns, max	Data Hold time after $\overline{RD}$ (bus relinquish time)
t_{17}	0	0	0	ns, min	$\overline{RD}$ to $\overline{CS}$ Hold time
t_{18}	0	0	0	ns, min	$\overline{RD}$ to $\overline{HBEN}$ Hold time
RESET TIMING					
t_{19}	60	70	80	ns, max	Data Ready low delay from $\overline{Reset}$
t_{20}	70	81	95	ns, max	Status low delay from $\overline{Reset}$

*Same specs as ADC700JH, AH, RH.

NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) See Table I. USB – Unipolar Straight Binary; BTC – Binary Two's Complement; BOB – Bipolar Offset Binary; NRZ – Non Return to Zero. (5) Max supply current is specified at rated supply voltages. (6) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. (7) t_{13} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. (8) t_{16} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$ to Digital Common ..... 0V to +7V
$+V_{CC}$ to Analog Common ..... 0V to +18V
$-V_{CC}$ to Analog Common ..... 0V to –18V
Digital Common to Analog Common ..... –1V to +1V
Digital Inputs to Digital Common ..... –0.5V to V_{DD} + 0.5V
Analog Inputs ..... +16.5V
Power Dissipation 1000mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature, (soldering, 10s) ..... +300°C

NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

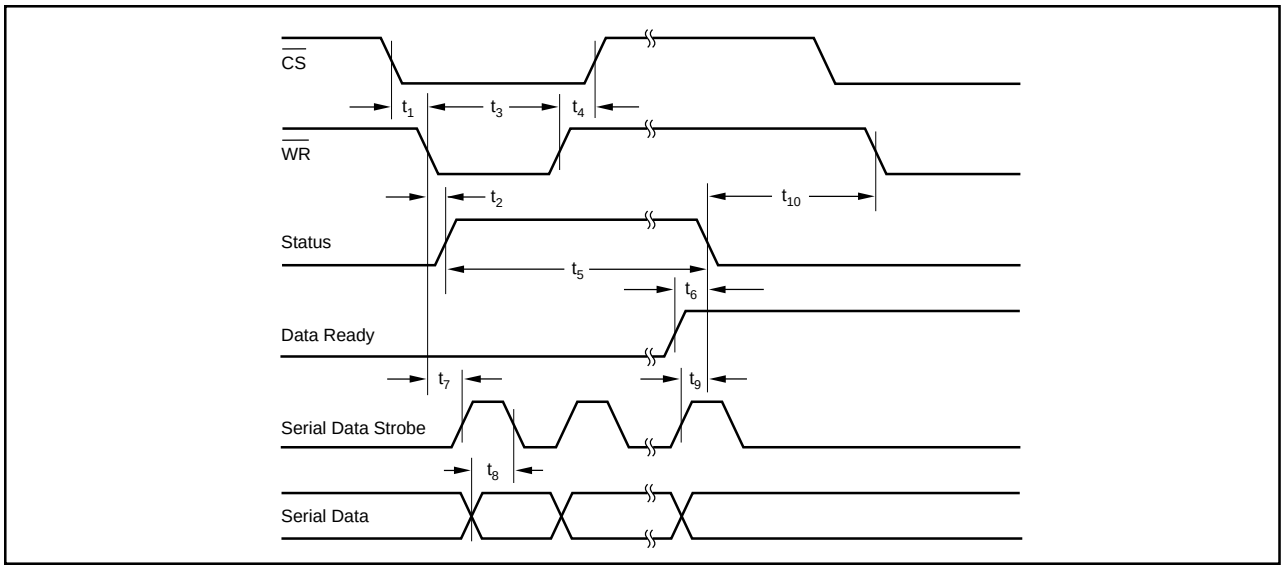
PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADC700JH	28-Pin Ceramic DIP	237
ADC700KH	28-Pin Ceramic DIP	237
ADC700AH	28-Pin Ceramic DIP	237
ADC700BH	28-Pin Ceramic DIP	237
ADC700RH	28-Pin Ceramic DIP	237
ADC700SH	28-Pin Ceramic DIP	237

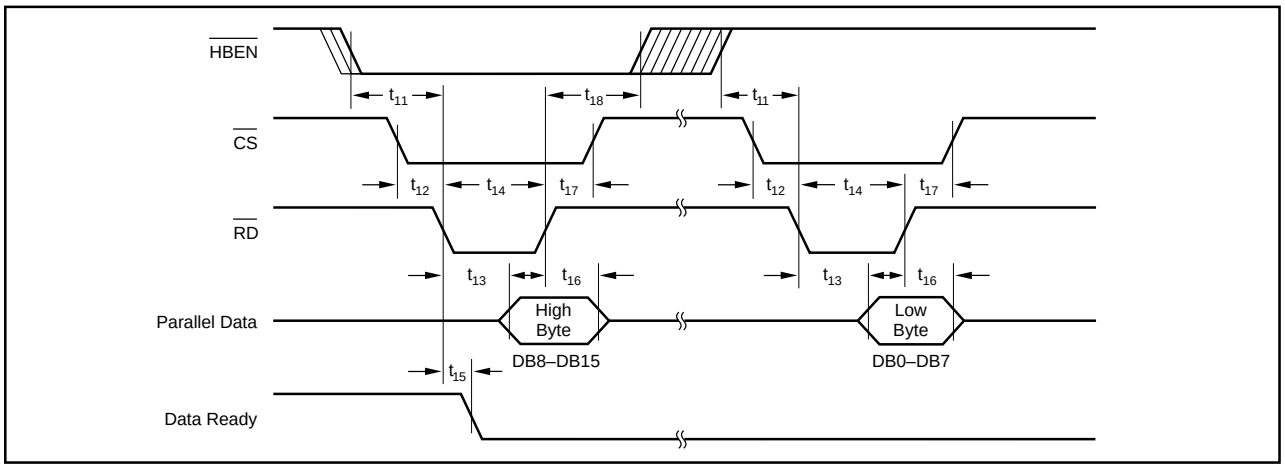
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

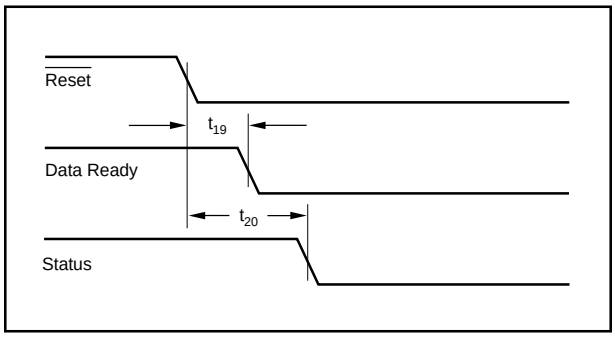
MODEL	TEMPERATURE RANGE	LINEARITY ERROR (%FSR)
ADC700JH	0°C to 70°C	±0.006
ADC700KH	0°C to 70°C	±0.003
ADC700AH	–25°C to +85°C	±0.006
ADC700BH	–25°C to +85°C	±0.003
ADC700RH	–55°C to +125°C	±0.006
ADC700SH	–55°C to +125°C	±0.003



Start of Conversion and Serial Data Output Timing.



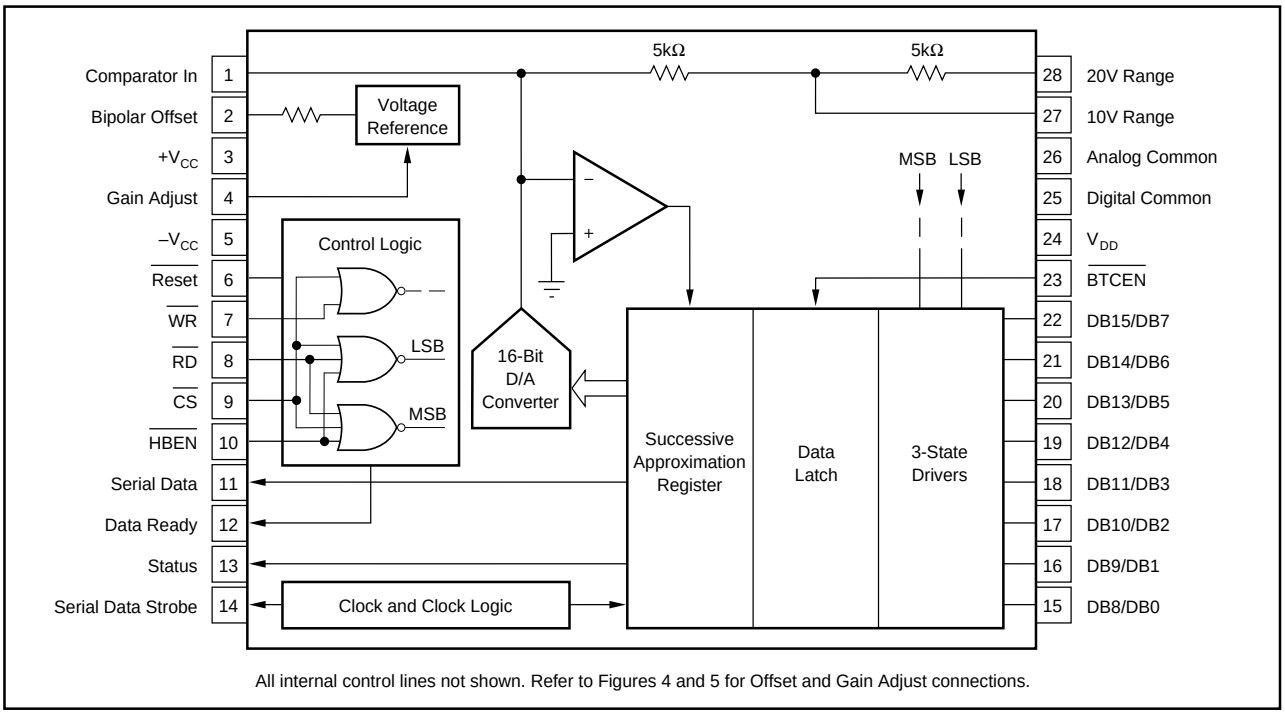
ADC700 Parallel Output Timing.



ADC700 Reset Function Timing Diagram.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



All internal control lines not shown. Refer to Figures 4 and 5 for Offset and Gain Adjust connections.

DESCRIPTION AND OPERATING FEATURES

The ADC700 is a 16-bit resolution successive approximation A/D converter. Parallel digital data as well as serial data is available. Several features have been included in the ADC700 making it easier to interface with microprocessors and/or serial data systems. Several analog input ranges are available.

Some of the key operating features are described here. More detail is given in later sections of the data sheet. Refer to the block diagram above.

RESET

The ADC700 has a $\overline{\text{Reset}}$ input that must be asserted upon power-up or after a power interruption. This initializes the SAR, the output buffer register and Data Ready flag. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700.

PARALLEL DATA

The parallel data output is available through an 8-bit port with 3-state output drivers. High byte and low byte are selected by $\overline{\text{HBEN}}$ (pin 10).

A buffer/latch is included between the successive approximation register (SAR) and the 3-state drivers. This feature permits more flexible interface timing than is possible from most successive approximation converters.

The "old" word can be read during the next conversion. A Data Ready flag (pin 12) is asserted when a "new" word is in the buffer register. The Data Ready flag goes low ("0") when the most significant byte (high byte) is read. If the "old" word is not read, or if only the least significant byte (low byte) is read, Data Ready is not reset. The next conversion output will overwrite the data latch when the conversion is complete. The Data Ready flag remains high. Refer to timing diagrams in the Specifications section.

SERIAL DATA

Sixteen-bit serial data output is available (pin 11) along with a serial output strobe (pin 14). This serial data strobe is not the internal SAR clock but is a special strobe for serial data consisting of 16 negative-going edges (during conversion) occurring about 200ns after each serial data bit is valid. This feature eases the interface to shift registers or through opto-couplers for applications requiring galvanic isolation.

STATUS

The familiar Status (or Busy) flag, present in successive approximation A/D converters, is available (pin 13) and indicates that a conversion is in progress. Status is valid 110ns after assertion of the convert command ($\overline{\text{WR}}$ low). Status cannot be used as a sample-hold control because there is not enough time for the sample-hold to settle to the required error band before the ADC700 makes its first conversion decision.

CHIP SELECT

$\overline{\text{CS}}$ (pin 9) selects the ADC700. No other functions can be implemented unless $\overline{\text{CS}}$ is asserted. $\overline{\text{WR}}$ (pin 7) is the start-of-conversion strobe. $\overline{\text{RD}}$ strobes each output data byte, selected by $\overline{\text{HBEN}}$ (pin 10), to the 3-state drivers.

TWO'S COMPLEMENT DATA CODE

$\overline{\text{BTCEN}}$ (pin 23) is a logic function that implements the Binary Two's Complement output code for bipolar (+ and –) analog input signal operation. This feature is compatible with twos complement arithmetic in microprocessor math algorithms.

INTERNAL CLOCK

The ADC700 has a self-contained clock to sequence the A/D logic. The clock is not available externally. An external 16-pulse strobe (pin 14) is brought out to clock serial data only. Use of ADC700 with external clock is not possible.

INTERNAL VOLTAGE REFERENCE

The ADC700 has an internal low-noise buried-zener voltage reference. The reference circuit has been drift compensated over the MIL temperature range using a laser trim algorithm. The reference voltage is not available externally.

DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Refer to Figure 3 for an illustration of A/D converter terminology and to Table II in the Calibration section.

Full Scale Range, FSR

The nominal range of the A/D converter. For ADC700, the FSR is 20V for the 0V to +20V and the –10V to +10V input ranges or 10V for the 0V to +10V and –5V to +5V input ranges.

Least Significant Bit, LSB

The smallest analog input change resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is FSR(2^{-N}).

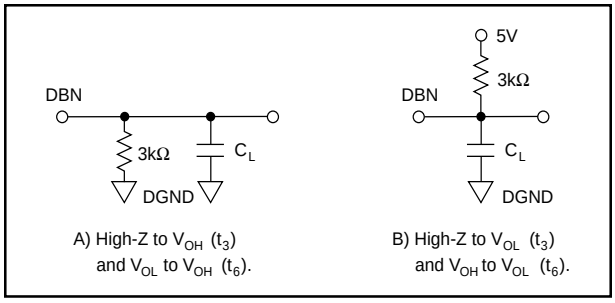


FIGURE 1. Load Circuits for Access Time.

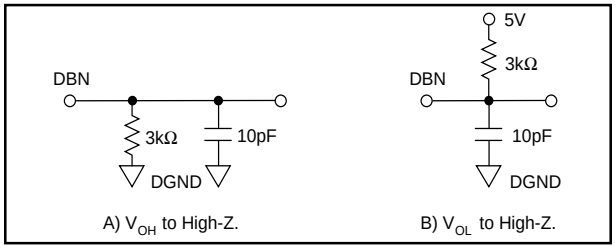


FIGURE 2. Load Circuits for Output Float Delay.

Most Significant Bit, MSB

That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution

An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

ACCURACY

Linearity Error, Integral Linearity Error (ILE)

Linearity Error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near positive full scale (at $+V_{FS}$ –1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at Zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$). Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADC700KH ILE is ±0.003% of FSR which is 1/2 LSB at 14-bits.

Differential Linearity Error (DLE), No Missing Codes

Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADC700KH is specified to have a DLE of ±0.006% of FSR, which is ±1LSB at 14 bits. ADC700KH is specified to have *no missing codes* at the 14-bit level over specified temperature ranges.

Gain Error

The deviation from the ideal magnitude of the input span between the first code midpoint (at $-V_{FS}$ + 1/2LSB, for bipolar operation; at Zero for unipolar operation) to the last code midpoint (V_{FS} –1LSB). As with the linearity error

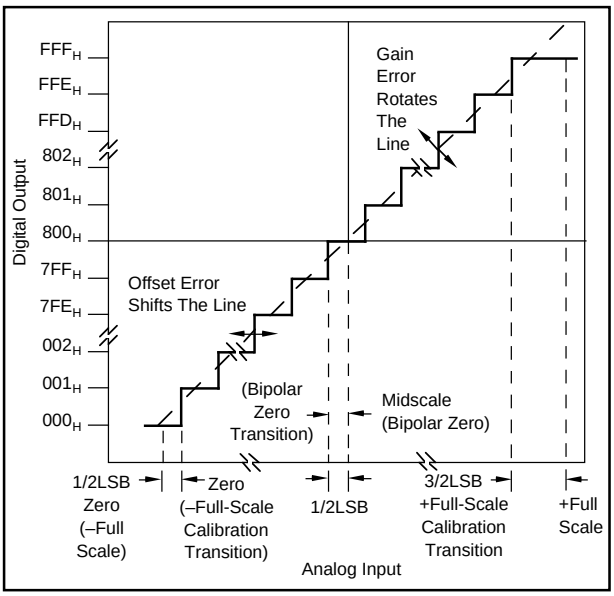


FIGURE 3. Transfer Characteristic Terminology.

measurements, code transition values are the locations actually measured for this spec. The ideal gain is V_{FSR} –2LSB. Gain Error is expressed in % (of reading). See Figure 3.

Gain Error of the ADC700 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error—The deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error—The deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at – V_{FS} +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADC700 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a percentage of FSR.

Bipolar Zero Error—The deviation of the actual mid-scale-code midpoint value from zero. Transition values are the actual measured parameter and it is 1/2 LSB below zero volts. The error is comprised of Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error of bit 1. Bipolar Zero Error is expressed as a percentage of FSR.

Power Supply Sensitivity

Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. PSR is specified in units of %FSR/% change in each supply voltage.

The major effect of power supply voltage deviations from the rated values will be a small change in the Gain (scale factor). Power Supply Sensitivity is also a function of ripple frequency. Figure 4 illustrates typical Power Supply Sensitivity performance of ADC700 versus ripple frequency.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADC700, system design problems such as ground path resistance and contact resistance become very important. For a 16-bit resolution converter with a +10V Full-Scale Range, 1LSB is 153µV. Circuit situations that cause only second- or third-order errors in 8-, 10-, or 12-bit A/D converters can induce first-order errors in 16-bit resolution devices.

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the analog and digital common lines.

Power Supply Returns (Analog Common and Digital Common)

Connect Analog Common and Digital Common together right at the converter with the ground plane. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. Connect a 1 to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing

Every power-supply line leading into an A/D converter must be bypassed to its common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 10µF to 100µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals

Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Shield Other Sensitive Points

The most critical of these is the comparator input (pin 1). If this pin is not used for offset adjustment, then it should be surrounded with ground plane or low-impedance power

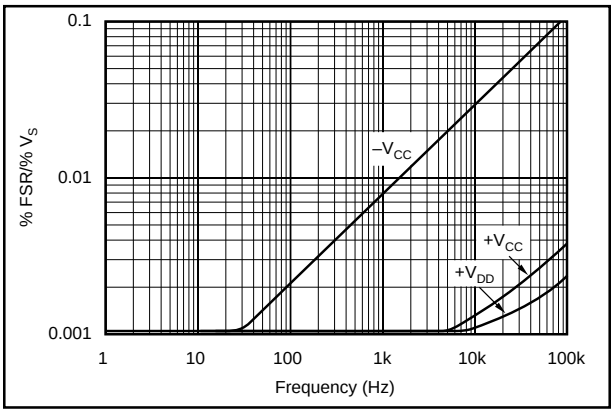


FIGURE 4. Power Supply Rejection Ripple vs Frequency.

supply plane. If it is used for offset adjustment, the series resistor and potentiometer should be located as close to the converter as possible.

The Gain Adjust (pin 4) is an input that has a relatively high input impedance and is susceptible to noise pickup. The Gain Adjust pin should be bypassed with a 0.01µF to 0.1µF capacitor whether or not the gain adjust feature is used.

If the 20V Analog input range is used (pin 28), the 10V Range input (pin 27) may need to be shielded with ground plane to reduce noise pickup.

ANALOG SIGNAL SOURCE IMPEDANCE

The input impedance of the ADC700, typical of most successive approximation A/D converters, is relatively low (2.5kΩ to 10kΩ). The input current of a successive approximation A/D converter changes rapidly during the conversion algorithm as each bit current is compared to the analog input current. Since the output impedance of a closed-loop amplifier or a sample-hold amplifier increases with frequency and, in addition, the amplifier must settle to the required accuracy in time for the next comparison/ decision after such a disturbance, care must be taken to select the proper driving amplifier.

Unfortunately, high-accuracy operational amplifiers tend to have low bandwidth, while wide-band amplifiers tend to have lower accuracy. One solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a wide-band buffer amplifier such as the Burr-Brown OPA633 inside the feedback loop of a slower (but precision) amplifier, Figure 5. This reduces the output impedance at high frequencies yet preserves the accuracy at low frequencies. When a sample/hold is needed, a high-linearity, high-speed sample/hold such as the Burr-Brown SHC76 should be used to drive the ADC700.

ANALOG INPUT RANGES

The analog input circuits of the ADC700 can be connected to accept unipolar or bipolar input signals. These ranges and connections are tabulated in Table I. Circuit connections are shown in Figures 6 and 7. Gain and offset adjustments are described in the calibration section.

To operate the ADC700 with a range that gives other convenient values for the LSB, the input resistor may be increased or decreased slightly without seriously affecting the Gain Drift of the converter. Since the input resistors of the ADC700 are within ±2% from unit to unit, this can be consistently done with a fixed series or parallel resistor. The ADC700 can then be calibrated using the Gain and Offset adjustments described in the calibration section. For example, using the ±10V input range, one can decrease the range slightly by paralleling the 10kΩ input resistor (pin 28 to pin 1) with a 610kΩ metal film resistor to achieve a 300µV LSB instead of the nominal standard 305.17578µV binary LSB.

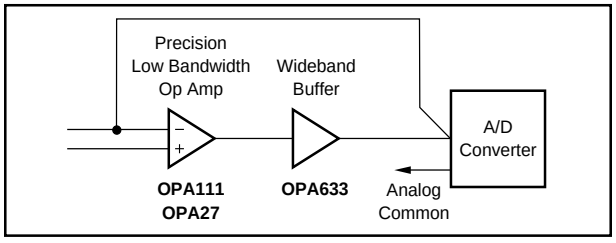


FIGURE 5. Wideband Buffer Reduces Output Impedance at High Frequencies.

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Gain and Offset Error may be trimmed to zero using external Gain and Offset trim potentiometers connected to the ADC700 as shown in Figures 6 and Figure 7. A calibration procedure in described in the Operating Instructions section.

Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature. These potentiometers may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 1 (Comparator In) and pin 4 (Gain Adjust) may be left open if no external adjustment is planned; however, pin 4 should always be bypassed with 0.01µF or larger to Analog Common.

OPERATING INSTRUCTIONS

CALIBRATION

Offset and Gain may be trimmed by external Offset and Gain potentiometers. Offset is adjusted first and then Gain. Calibration values are listed in Table II for all ADC700 input ranges. Offset and Gain calibration can be accomplished to a precision of about ±1/2LSB using a static adjustment procedure described below. By summing a small sine or triangular wave voltage with the accurate calibration voltage applied to the analog input, the output can be swept through each of the calibration codes to more accurately determine the transition points listed in Table II. NOTE: The transition points are not the same as the code midpoints used in the static calibration example.

OFFSET ADJUSTMENT, 14-BIT RESOLUTION EXAMPLE

Static Adjustment Procedure (At Code Midpoints)

0V to +10V Range—Set the analog input to $+1LSB_{14}$ = 0.00061V. Adjust the Offset potentiometer for a digital output of 0004_H. Set the analog input to +Full Scale – $2LSB_{14}$ = +9.9987V. Adjust the Gain potentiometer for a digital output of $FFFC_H$. For a half-scale calibration check, set the analog input to +5.0000V and read a digital output code of 8000_H.

INPUT SIGNAL RANGE	OUTPUT CODE		CONNECT PIN 2 TO PIN	CONNECT PIN 28 TO PIN	CONNECT SIGNAL TO PIN
	$\overline{BTCEN}$ = 1	$\overline{BTCEN}$ = 0			
±10V	BOB	BTC	1	Input Signal	28
±5V	BOB	BTC	1	Open	27
±2.5V	BOB	BTC	1	Pin 1	27
0V to +5V	USB	—	26	Pin 1	27
0V to +10V	USB	—	26	Open	27
0V to +20V	USB	—	26	Input Signal	28

TABLE I. ADC700 Input Range Connections.

ANALOG INPUT RANGE	VOLTAGE (V)					
	±10	±5	±2.5	0 TO +20	0 TO +10	0 TO +5
$+V_{FS}$	+10	+5	+2.5	+20	+10	+5
$-V_{FS}$	–10	–5	–2.5	0	0	0
FSR	20	10	5	20	10	5
TRANSITION CODES (Hexadecimal)	**TRANSITION VALUES (V)**					
For 16-bit Resolution (Reading all 16 bits)						
$FFFE_H$ to $FFFF_H$	+9.999542	+4.999771	+2.499886	+19.999542	+9.99971	+4.999886
$7FFF_H$ to 8000_H	–152.5µV	–38µV	–19µV	+9.999847	+4.999924	+2.499962
0000_H to 0001_H	–9.999847	–4.999924	–2.499962	+152µV	+76µV	+38µV
LSB (FSR/2^{16})	305µV	153µV	38µV	305µV	153µV	76µV
For 15-bit Resolution (Reading all 16 bits, Ignoring DB_0)						
$FFFD_H$ to $7FFE_H$	+9.999084	+4.999542	+2.499771	+19.999084	+9.999542	+4.999771
$7FFE_H$ to 8000_H	–305µV	–153µV	–76µV	+9.999625	+4.999847	+2.499924
0000_H to 0002_H	–9.999695	–4.999847	–2.499924	+305µV	+152µV	+76µV
LSB (FSR/2^{15})	610µV	305µV	153µV	610µV	305µV	153µV
For 14-bit Resolution (Reading all 16 bits, Ignoring DB_0 and DB_1)						
$FFFC_H$ to $FFFD_H$	+9.99817	+4.99908	+2.49954	+19.99817	+9.99908	+4.99954
$7FFD_H$ to 8000_H	–610µV	–305µV	–153µV	+9.99939	+4.999695	+2.499847
0000_H to 0004_H	–9.999390	–4.999694	–2.499847	+610µV	+305µV	+153µV
LSB (FSR/2^{14})	1221µV	610µV	305µV	1221µV	610µV	305µV

TABLE II. Transition Values for Calibration.

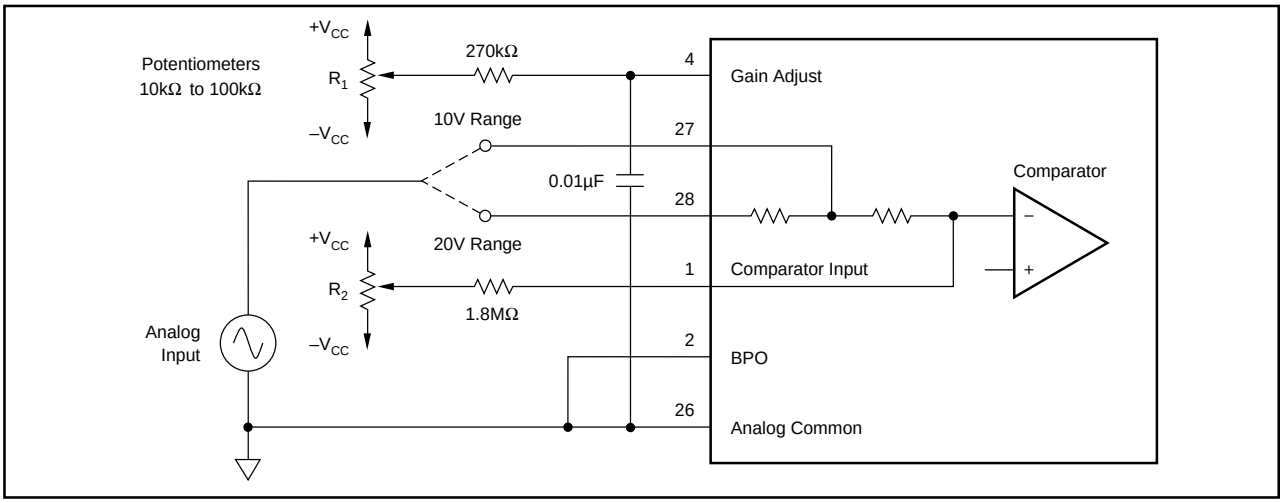


FIGURE 6. Unipolar Input Configuration with Gain and Offset Adjust Connections.

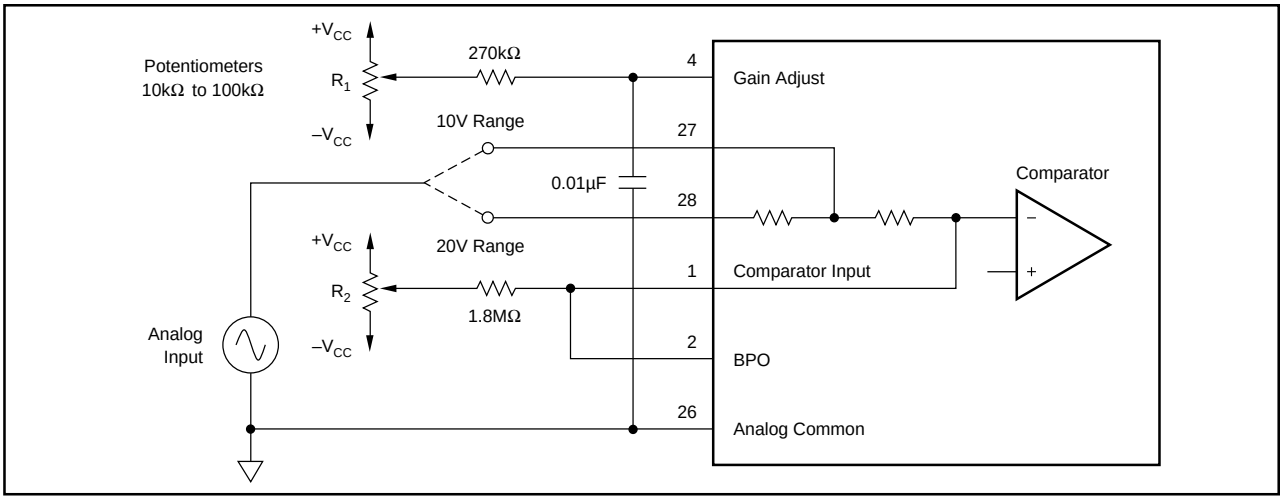


FIGURE 7. Bipolar Input Configuration with Gain and Offset Adjust Connections.

–10V to +10V Range—Set the analog input to –FS + $1LSB_{14}$ = –9.99878V. Adjust the Offset potentiometer for a digital output of 0004_H (8004_H if $\overline{BTCEN}$ is asserted). Set the analog input to +9.9976V. Adjust the Gain potentiometer for a digital output of $FFFC_H$ ($7FFC_H$ if $\overline{BTCEN}$ is assrted). For a half-scale calibration check, set the analog input to 0.0000V and read a digital output code of 8000_H (0000_H if $\overline{BTCEN}$ is asserted).

CONTROLLING AND INTERFACING THE ADC700

RESET

The ADC700 requires a Reset command upon power-up or after a power interruption to guarantee the condition of internal registers. If Status powers-up High, no conversion can be started. Reset initializes the SAR, the output buffer register, and the Data Ready flag and terminates a conversion in progress. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700. A power-up circuit is shown in Figure 8. Refer to Reset function timing diagram following the Timing Specifications Table.

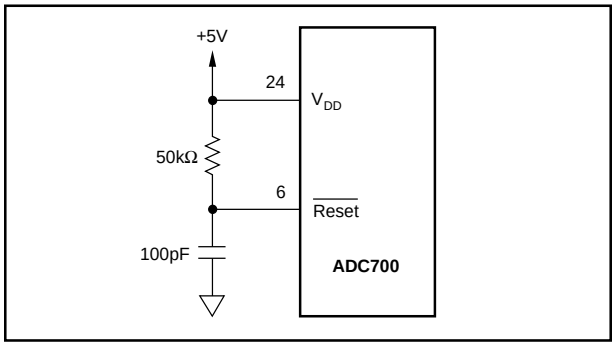


FIGURE 8. Power-Up Reset Circuit.

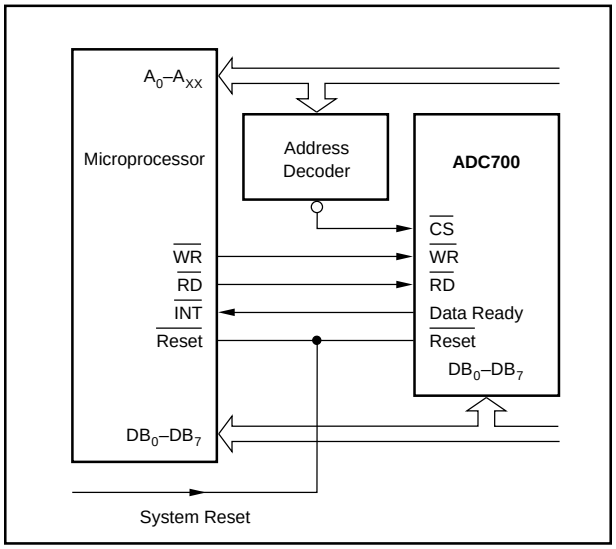


FIGURE 9. Parallel Data Bus Interface.

START OF CONVERSION

A conversion is started by asserting $\overline{CS}$ and $\overline{WR}$ Low. Status goes high about $t = t_1 + t_2$ = 110ns later. The first successive approximation decision occurs about 900ns after $\overline{WR}$ is asserted. Status goes Low after the conversion is complete. Refer to Start of Conversion and Serial Data Output Timing following the Timing Specifications Table.

DATA READY FLAG

The data latch feature permits data to be read during the following conversion. The Data Ready flag indicates that the data from the most recent conversion is latched in the output data latch and that it hasn't been read. Data Ready remains High until the most significant data byte is read. If a subsequent conversion is initiated and completed, the new word will be stored in the output data latch regardless of the state of the Data Ready flag. The preceding word will be overwritten and lost.

READING PARALLEL DATA

Parallel data is latched in the output data latch at the end of a conversion. Data can be read any time, even during the subsequent conversion. The output data latch is not cleared by reading the data. Only the Data Ready flag is cleared by reading the MSB.

The output three-state drivers are enabled by asserting the $\overline{CS}$ and $\overline{RD}$ inputs Low. When $\overline{HBEN}$ is Low, the most significant eight bits are enabled and the Data Ready flag is cleared. When $\overline{HBEN}$ is High, the least significant eight bits are enabled. Refer to Parallel Data Output Timing information following the Timing Specifications Table.

To reduce noise interference to the absolute minimum, data should be read after the current conversion is complete. However, data can be read during the following conversion, with minimal interference, to maximize the sampling rate of the converter.

A typical parallel interface is illustrated in Figure 9.

READING SERIAL DATA

Serial data output of the ADC700 is facilitated by a Serial Data Strobe that provides 16 negative-going edges for strobing an external serial to parallel shift register located perhaps on the other side of an opto-coupler. Refer to the Serial Data Timing information following the Timing Specifications Table. An example of an isolation connection using the serial port feature is illustrated in Figure 10.

CONTINUOUS CONVERSION OPERATION

When $\overline{CS}$ is permanently connected to Digital Common and Status is connected to $\overline{WR}$, Figure 11, the ADC700 will continuously convert. The repetition time will not be precise and will vary slightly with the temperature for the ADC700 because the time will be determined by the internal clock frequency and control-circuit gate delays. If a precise repetition rate is needed, the continuous conversion connection should not be used.

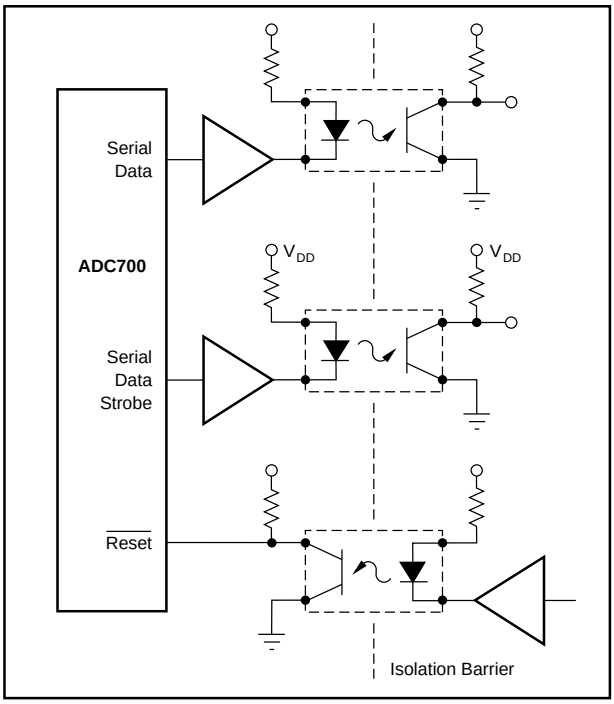


FIGURE 10. Serial Data Output Providing Convenient Isolation.

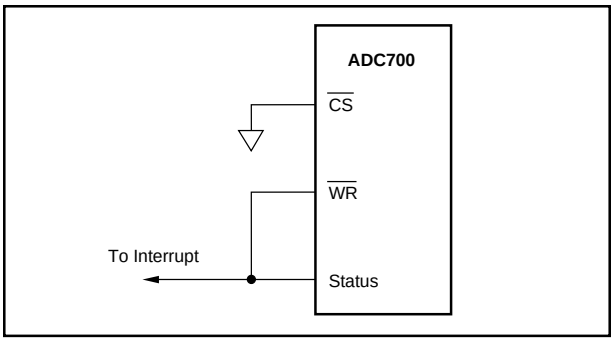


FIGURE 11. Continuous Conversion Circuit Connection.

PIN DESIGNATION	DEFINITION	FUNCTION
$\overline{CS}$ (Pin 9)	Chip Select	Must be Low to either initiate a conversion or read output data.
$\overline{WR}$ (Pin 7)	Write (Convert)	Conversion begins after the High-to-Low transition.
$\overline{RD}$ (Pin 8)	Read	Turns ON the three-state output drivers upon being asserted low.
$\overline{HBEN}$ (Pin 10)	High Byte Enable "1" = Low Byte "0" = High Byte	Selects the MSB or the LSB for readout. Data Ready is cleared when $\overline{HBEN}$ is Low and $\overline{RD}$ is asserted.
$\overline{Reset}$ (Pin 6)	Reset	Resets internal logic. Must be asserted after power-up or a power interruption clears Status and Data Ready to Low.
$\overline{BTCEN}$ (Pin 23)	BTC Enable	Sets the output code to Binary Twos Complement (BTC) when Low. Output code is Bipolar Offset Binary (BOB) when High.

TABLE III. Control Line Functions.

CONTROL LINE					
$\overline{RESET}$	$\overline{WR}$	$\overline{RD}$	$\overline{HBEN}$	$\overline{CS}$	OPERATION
0	X	X	X	X	Reset converter logic. Status and Data Ready set Low.
1	X	X	X	1	No operation.
1	0	X	X	0	Initiate conversion.
1	1	0	0	0	Places High Byte on output port. Clears Data Ready flag.
1	1	0	1	0	Placed Low Byte on output port. Does not clear Data Ready flag.
1	0	0	0	0	Initiates conversion and places High Byte or output port. Clears Data Ready.
1	0	0	1	0	Initiates conversion and places Low Byte on output port. Does not clear Data Ready flag.

NOTE: If a conversion command is asserted while a conversion is in progress, the command is ignored. If the conversion command remains asserted when a conversion is finished, a new conversion will begin.

TABLE IV. Control Input Truth Table.

Because the last data-word is stored in the data latch, it is possible to read it during the next A/D conversion. Assertion of $\overline{CS}$ and $\overline{HBEN}$ for reading parallel data should be timed from Status going low. The two-byte read operation must be complete before the conversion in process is complete or the Data Read is invalid.

Serial Data is available during continuous conversion with word synchronization available from STATUS.

USING A SAMPLE/HOLD WITH ADC700

Figure 12 illustrates using ADC700 with the Burr-Brown SHC76. The sample-to-hold settling time (to 14 bits, ±0.003%FSR) of the SHC76 is 1µs typ, 3µs max. The time from the Status going High to the first conversion decision is about 900ns. Therefore a time delay between the Sample-to-Hold command to the $\overline{WR}$ command to the ADC700 is required.

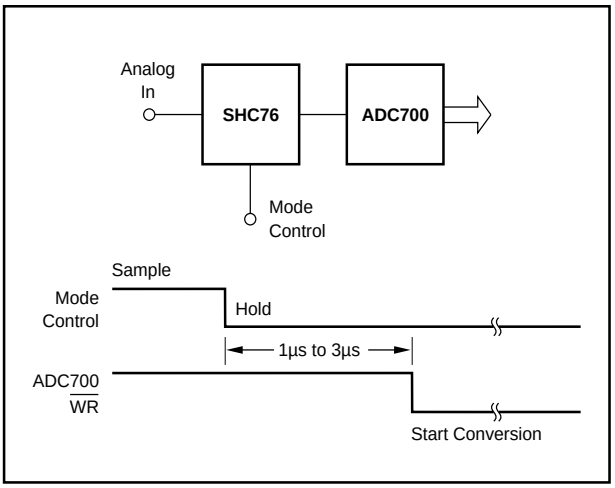


FIGURE 12. Using Sample/Hold with ADC700 Requires Time Delay Between Sample and Start-of-Conversion.