MultiPort Internet Gateway Processor

ADSP-21mod980

FEATURES

PERFORMANCE

- Complete Single-Chip MultiPort Internet Gateway Processor (No External Memory Required)
- Implements Sixteen Modem Channels or Forty Voice Channels in One Package
- Each Processor Can Implement One V.34/V.90 Data/Fax Modem (Includes Datapump and Controller)
- Standard Power Version: 600 MIPS Sustained Performance, 13.3 ns Instruction Time @ 2.75 V (Internal)
- Low Power Version: 600 MIPS Sustained Performance, 13.3 ns Instruction Time @ 1.80 V (Internal)
- Open Architecture Extensible to Voice-over-Network (VoN) and Other Applications
- Low Power Dissipation, 45 mW (Typical) Per Channel
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation

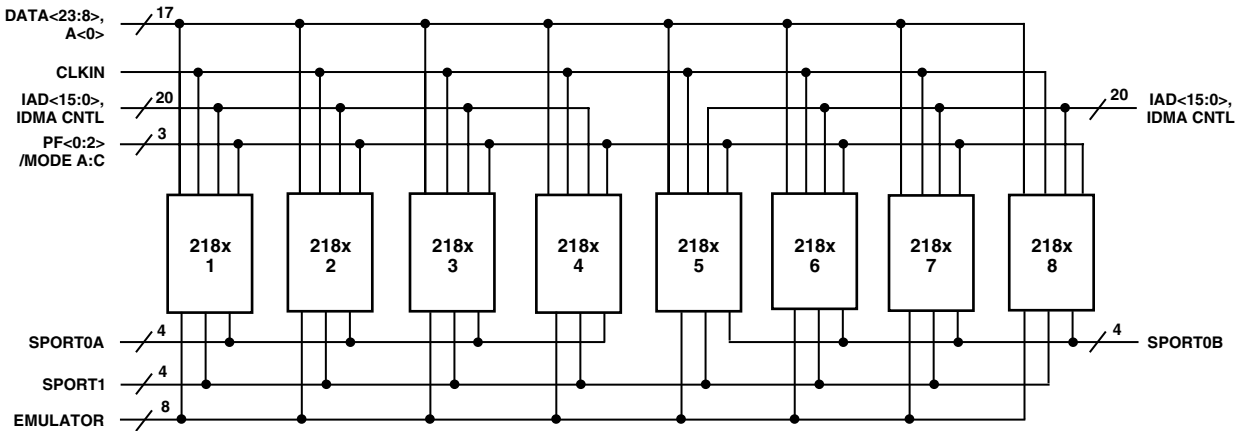
INTEGRATION

- ADSP-2100 Family Code-Compatible, with Instruction Set Extensions
- 2.00M Bytes of On-Chip SRAM, Configured as 1.125M Bytes of Program Memory and 0.875M Bytes of Data Memory
- Dual-Purpose Program Memory, for Both Instruction and Data Storage
- 352-Ball PBGA with a 1.9 Square Inch (1225 Square mm) Footprint

SYSTEM CONFIGURATION

- 16-Bit Internal DMA Port for High-Speed Access to On-Chip Memory (Mode-Selectable)
- Programmable Multichannel Serial Port Supports 24/32 Channels
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Separate $\overline{\text{RESET}}$ Pins for Each Internal Processor

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The ADSP-21mod980 is a multiport Internet gateway processor optimized for implementation of a complete V.34/56K modem. All data pump and controller functions can be implemented on a single device, offering the lowest power consumption and highest possible modem port density.

The ADSP-21mod980 combines the ADSP-2100 Family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-21mod980 integrates 2.0M bytes of on-chip memory, configured as 384K words (24-bit) of program RAM, and 448K words (16-bit) of data RAM. Power-down circuitry is also provided to reduce the average and standby power consumption of equipment which, in turn, reduces equipment cooling requirements. The ADSP-21mod980 is available in a 35 sq-mm., 352-lead PBGA package.

Fabricated in a high-speed, low-power, CMOS process, the ADSP-21mod980 operates with a 13.3 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-21mod980's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-21mod980 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

Modem Software

The modem software executes general modem control, command sets, error correction and data compression, data modulations (for example, V.90 and V.34), and host interface functions. The host interface allows system access to modem statistics, such as call progress, connect speed, retrain count, symbol rate, and other modulation parameters.

The modem data pump and controller software resides in on-chip SRAM and does not require additional memory. The ADSP-21mod980 can be dynamically configured by downloading software from the host through the 16-bit DMA interface. This SRAM-based architecture provides a software upgrade path to other applications, such as Voice-Over-IP (VOIP), and to future standards. The modem software is available as object code.

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-21mod980. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

A PROM Splitter generates PROM programmer-compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-21mod980 assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-21mod980 system. The EZ-ICE, in conjunction with the required processor selection hardware, allows the user to independently debug code on individual modem processors. The emulator consists of hardware, host computer resident software, and target board connector. The ADSP-21mod980 integrates on-chip emulation support with a 14-pin ICE-Port interface. The ADSP-21mod980 device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See "Designing An EZ-ICE-Compatible Target System" in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections), as well as the Designing an EZ-ICE Compatible System section of this data sheet, for the exact specifications of the EZ-ICE target board connector.

Additional Information

This data sheet provides a general overview of ADSP-21mod980 functionality. For specific information about the modem processors, refer to the ADSP-2188M Preliminary data sheet. For additional information on the architecture and instruction set of the modem processors, refer to the *ADSP-2100 Family User's Manual,* Third Edition. For more information about the development tools, refer to the *ADSP-2100 Family Development Tools* data sheet.

EZ-ICE is a registered trademark of Analog Devices, Inc.

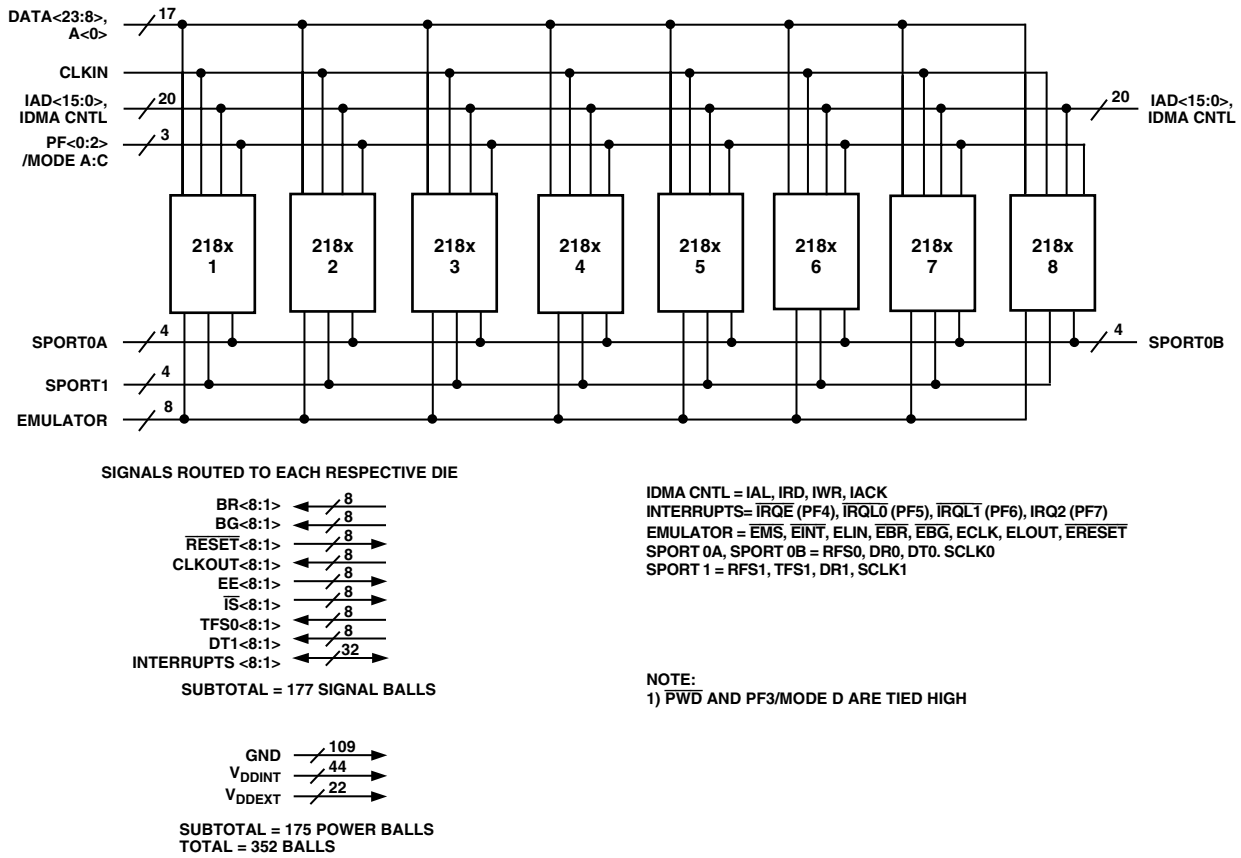


Figure 1. ADSP-21mod980 Processor Pool

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-21mod980 MultiPort Internet Gateway Processor. It contains eight independent digital signal processors.

Every modem processor has:

- A DSP core
- 256K bytes of RAM
- Two serial ports
- A DMA port

The signals of each modem processor are accessed through the external pins of the ADSP-21mod980. Some signals are bused with the signals of the other processors and are accessed through a single external pin. Other signals remain separate and are accessed through separate external pins for each processor.

The arrangement of the eight modem processors in the ADSP-21mod980 makes one basic configuration possible: a *slave* configuration. In this configuration, the data pins of all eight processors connect to a single bus structure.

All eight modem processors have identical functions and equal status. Each of the four modem processors are connected to a common DMA bus and each modem processor is configured to operate in the same mode (see the Slave Mode and the Memory Mode descriptions in the Memory Architecture section. The slave mode is considered to be the only mode of operation in the ADSP-21mod980 modem pool.

Serial Ports

The ADSP-21mod980 has a multichannel serial port (SPORT) connected to each internal digital modem processor for serial communications.

The following is a brief list of ADSP-21mod980 SPORT features. For additional information on the internal Serial Ports, refer to the *ADSP-2100 Family User's Manual.* Each SPORT:

- Is bidirectional and has a separate, double-buffered transmit and receive section.
- Can use an external serial clock or generate its own serial clock internally.
- Has independent framing for the receive and transmit sections. Sections run in a frameless mode, or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- Supports serial data word lengths from 3 to 16 bits and provides optional A-law and μ-law companding according to CCITT recommendation G.711.
- Receive and transmit sections can generate unique interrupts on completing a data word transfer.
- Can receive and transmit an entire circular buffer of data with one overhead cycle per data word. An interrupt is generated after a data buffer transfer.

A multichannel interface selectively receives and transmits a 24- or 32-word, time-division multiplexed, serial bitstream.

PIN DESCRIPTIONS

The ADSP-21mod980 is available in a 352-lead PBGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt, and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Common-Mode Pins

Pin Name(s)	# of Pins	Input/ Output	Function
$\overline{\text{RESET}}$	8	I	Processor Reset Input
$\overline{\text{BR}}$	8	I	Bus Request Input
$\overline{\text{BG}}$	8	O	Bus Grant Output
$\overline{\text{IRQ2}}$/	8	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O Pin
$\overline{\text{IRQL0}}$/	8	I	Level-Sensitive Interrupt Request[1]
PF5		I/O	Programmable I/O Pin
$\overline{\text{IRQL1}}$/	8	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{\text{IRQE}}$/	8	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
Mode C/	1	I	Mode Select Input—Checked Only
PF2			During $\overline{\text{RESET}}$
		I/O	Programmable I/O Pin During Normal Operation
Mode B/	1	I	Mode Select Input—Checked Only
PF1			During $\overline{\text{RESET}}$
		I/O	Programmable I/O Pin During Normal Operation
Mode A/	1	I	Mode Select Input—Checked Only
PF0			During $\overline{\text{RESET}}$
		I/O	Programmable I/O Pin During Normal Operation
CLKIN	1	I	Clock Input
CLKOUT	8	O	Processor Clock Output
SPORT	28	I/O	Serial Port I/O Pins[2]
V_{DD} and GND	175	I	Power and Ground
EZ-Port	16	I/O	For Emulation Use

NOTES

[1]Interrupt/Flag Pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the modem pool will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.

[2]SPORT configuration determined by the modem pool's System Control Register. Software configurable.

MEMORY INTERFACE PINS

The ADSP-21mod980 modem pool is used in slave mode. In slave mode, the modem processors operate in host configuration. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the modem pool is running. See the Memory Architecture section for more information.

Host Pins (Mode C = 1) Modem Processors 1–8

Pin Name(s)	# of Pins	Input/ Output	Function
IAD15:0	32	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access
D23:8	16	I/O	Data I/O Pins for Program, Data Byte and I/O Spaces
$\overline{\text{IWR}}$	2	I	IDMA Write Enable
$\overline{\text{IRD}}$	2	I	IDMA Read Enable
IAL	2	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	8	I	IDMA Select
$\overline{\text{IACK}}$	2	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

INTERRUPTS

The interrupt controller allows each modem processor in the modem pool to respond individually to 11 possible interrupts and reset with minimum overhead. The ADSP-21mod980 provides four dedicated external interrupt input pins, $\overline{\text{IRQ2}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQL0}}$, and $\overline{\text{IRQE}}$ (shared with the PF7:4 pins) for each modem processor. The ADSP-21mod980 also supports internal interrupts from the timer, the byte DMA port, the serial port, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ0}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{\text{IRQ2}}$	0004
$\overline{\text{IRQL1}}$	0008
$\overline{\text{IRQL0}}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{\text{IRQE}}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or IRQ1	0020
SPORT1 Receive or IRQ0	0024
Timer	0028 (Lowest Priority)

When the modem pool is reset, interrupt servicing is disabled.

LOW POWER OPERATION

The ADSP-21mod980 has three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-21mod980 modem pool has a low-power feature that lets the modem pool enter a very low-power dormant state through software control. Here is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The modem pool begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Power-down is initiated by the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down.
- Context clear/save control allows the modem pool to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.

Idle

When the ADSP-21mod980 is in the Idle Mode, the modem pool waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on the ADSP-21mod980 to let the modem pool's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

IDLE (*n*);

where *n* = 16, 32, 64, or 128. This instruction keeps the modem pool fully functional, but operating at the slower clock rate. While it is in this state, the modem pool's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (*n*) instruction is used, it effectively slows down the modem pool's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-21mod980 will remain in the idle state for up to a maximum of *n* modem pool cycles (*n* = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (*n*) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the modem pool's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the modem pool takes to come out of the idle state (a maximum of *n* cycles).

SYSTEM CONFIGURATION

Figure 2 shows the hardware interfaces for a typical multichannel modem configuration with the ADSP-21mod980. Other system design considerations, such as host processing requirements, electrical loading, and overall bus timing, must all be met. A line interface can be used to connect the multichannel subscriber or client data stream to the multichannel serial port of the ADSP-21mod980. The IDMA port of the ADSP-21mod980 is used to give a host processor full access to the internal memory of the ADSP-21mod980. This lets the host dynamically configure the ADSP-21mod980 by loading code and data into its internal memory. This configuration also lets the host access server data directly from the ADSP-21mod980's internal memory. In this configuration, the Modem Processors should be put into host memory mode where Mode C = 1, Mode B = 0, and Mode A = 1.

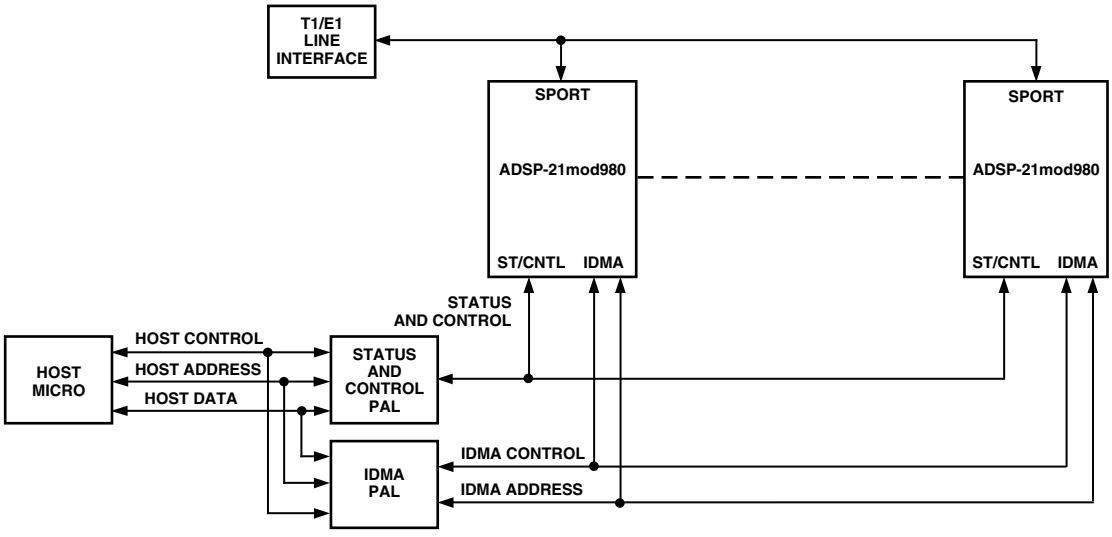


Figure 2. Multichannel Modem Configuration

CLOCK SIGNALS

The ADSP-21mod980 is clocked by a TTL-compatible clock signal that runs at half the instruction rate; a 37.5 MHz input clock yields a 13.3 ns processor cycle, which is equivalent to 75 MHz. Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled. The clock input signal is connected to the processor's CLKIN input.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual* for a detailed explanation of this power-down feature.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate.

Reset

The $\overline{\text{RESET}}$ signals initiate a reset of each modem processor in the ADSP-21mod980. The $\overline{\text{RESET}}$ signals must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to let the internal clocks stabilize. If $\overline{\text{RESET}}$s are activated any time after power up, the clocks continue to run and do not require stabilization time.

The power-up sequence is defined as the total time required for the oscillator circuits to stabilize after a valid V_{DD} is applied to the processors, and for the internal phase-locked loops (PLL) to lock onto the specific frequency. A minimum of 2000 CLKIN cycles ensures that the PLLs have locked, but this does not include the oscillators' start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signals should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signals must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ inputs contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signals, the use of external Schmitt triggers is recommended.

The reset for each individual modem processor sets the internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When a $\overline{\text{RESET}}$ is released, if there is no pending bus request and the modem processor is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

MEMORY ARCHITECTURE

The ADSP-21mod980 provides a variety of memory and peripheral interface options for Modem Processor 1. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the ADSP-21mod980.

The ADSP-21mod980 modem pool operates in one memory mode: Slave Mode. The following figures and tables describe the memory of the ADSP-21mod980:

- Figure 3 shows Program Memory.
- Figure 4 shows Data Memory.
- Table II explains the generation of address bits based on the PMOVLAY values.
- Table III explains the generation of address bits based on the DMOVLAY values. Access to external memory is not available.

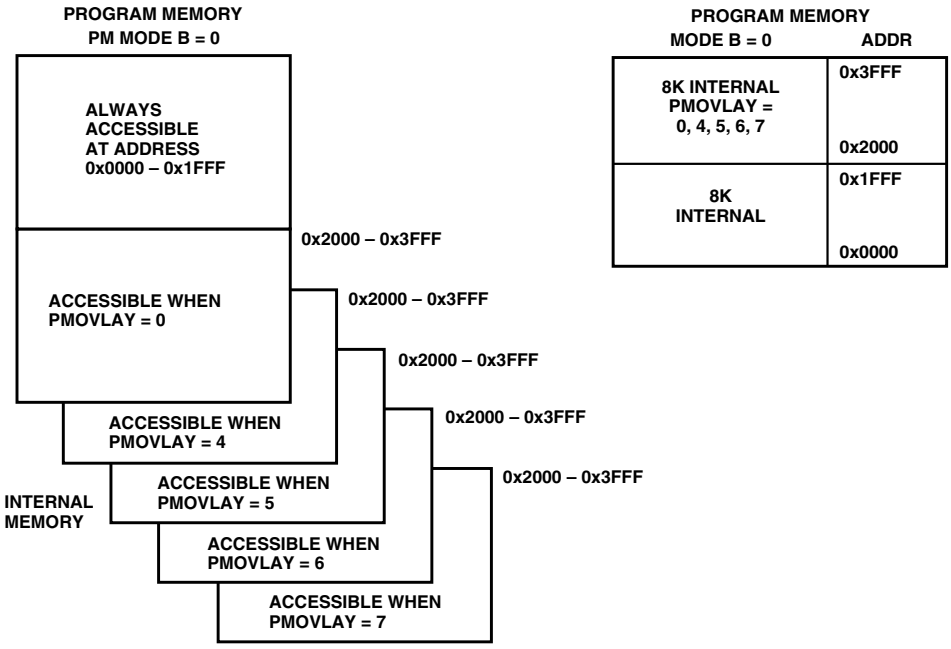


Figure 3. Program Memory

Table II. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0, 4, 5, 6, 7	Internal	Not Applicable	Not Applicable

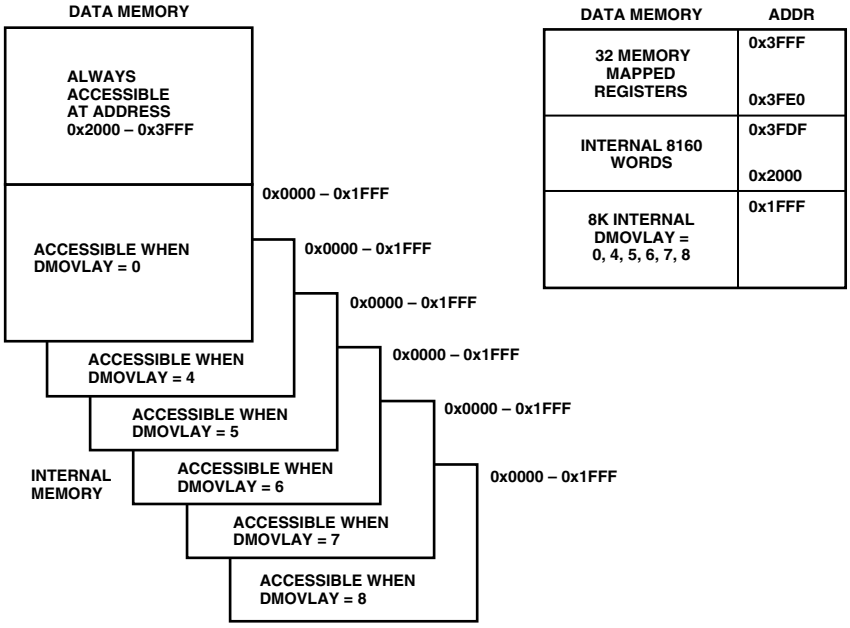


Figure 4. Data Memory Map

Table III. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0, 4, 5, 6, 7, 8	Internal	Not Applicable	Not Applicable

Memory-Mapped Registers (New to the ADSP-21mod980)
The ADSP-21mod980 has three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-21mod980's wait state and $\overline{\text{BMS}}$ control features.

Slave Mode
This section describes the Slave Mode memory configuration of the Modem Processors.

Internal Memory DMA Port (IDMA Port)
The IDMA Port provides an efficient way for a host system and the ADSP-21mod980 to communicate. The port is used to access the on-chip program memory and data memory of each modem processor with only one processor cycle per word overhead. The IDMA port cannot be used, however, to write to the processor's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the processor's IDMA control registers.

If IAD [15] = 1, the value of IAD [7:07] represents the IDMA overlay: IAD[14:8] must be set to 0.

If IAD [15] = 0, the value of IAD [13:0] represents the starting address of internal memory to be accessed and IAD [14] reflects PM or DM for access.

3. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) processor internal memory (PM or DM).
4. Host ends IDMA transfer.

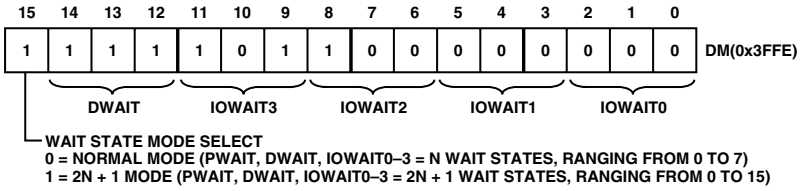


Figure 5. Wait State Control Register

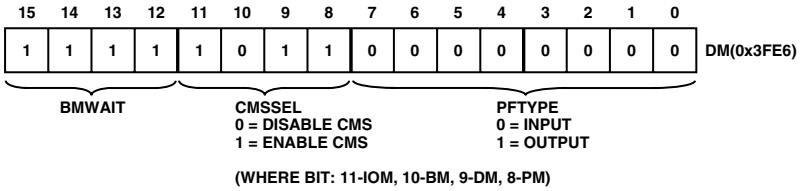


Figure 6. Programmable Flag and Composite Select Control Register

NOTE: Since they are multiplexed within the ADSP-21mod980, PF[2:0] should be configured as an output for only one processor at a time. Bit [3] of DM (0x3F36) must also be 0.

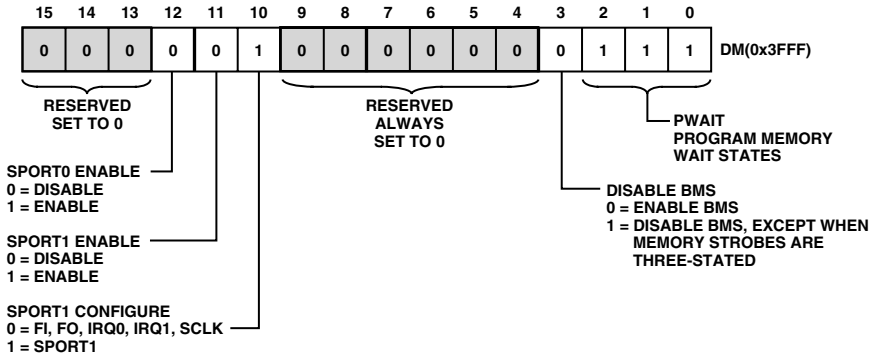


Figure 7. System Control Register

Table IV. ADSP-21mod980 Mode of Operation

MODE C	MODE B	MODE A	Booting Method
1	0	1	IDMA feature is used to load internal memory as desired. Program execution is held off until internal program memory location 0x0000 is written to. Chip is configured in Slave Mode.[1] $\overline{\text{IACK}}$ requires external pull-down.[1]

[1]Considered standard operating settings. These configurations simplify your design and improve memory management. IDMA timing details and the correct usage of $\overline{\text{IACK}}$ are described in the A*DSP-2100 Family User's Manual;* refer to pages 11-18 thru 11-19.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to, while the ADSP-21mod980 is operating at full speed.

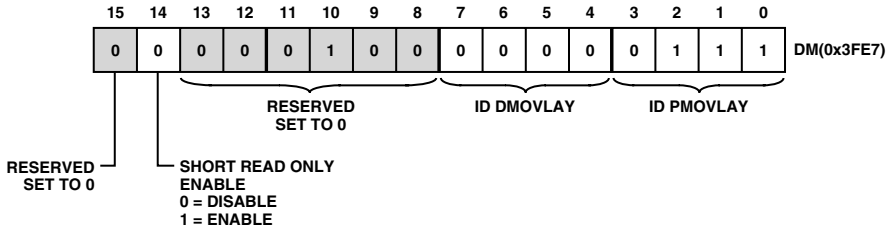
The processor memory address is latched and then automatically incremented after each IDMA transaction. An external device can, therefore, access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the *IDMA Address Latch cycle*. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

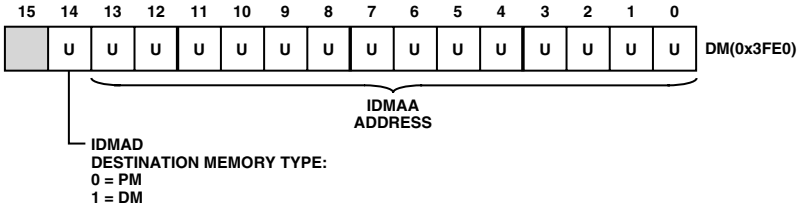
Once the address is stored, data can then be either read from, or written to, the ADSP-21mod980's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-21mod980 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the processor can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{IS}$) and address latch enable (IAL) directs the ADSP-21mod980 to write the address onto the IAD [14:0] bus into the IDMA Control Register. If IAD [15] is set to 0, IDMA latches the address. If IAD [15] is set to 1, IDMA latches OVLAY memory. The IDMAA register is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) or overlay register cannot be read back by the host. The IDMA OVERLAY register is memory mapped at address DM(0x3FE7). See Figure 8 for more information on IDMA memory mapping. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 25 applies for short reads. When Bit 14 in 0x3FE7 is set to zero short reads, use the timing shown in Figure 26.



a. IDMA Overlay



b. IDMA Control (U = Undefined at Reset)

Figure 8. IDMA Control/OVLAY Registers

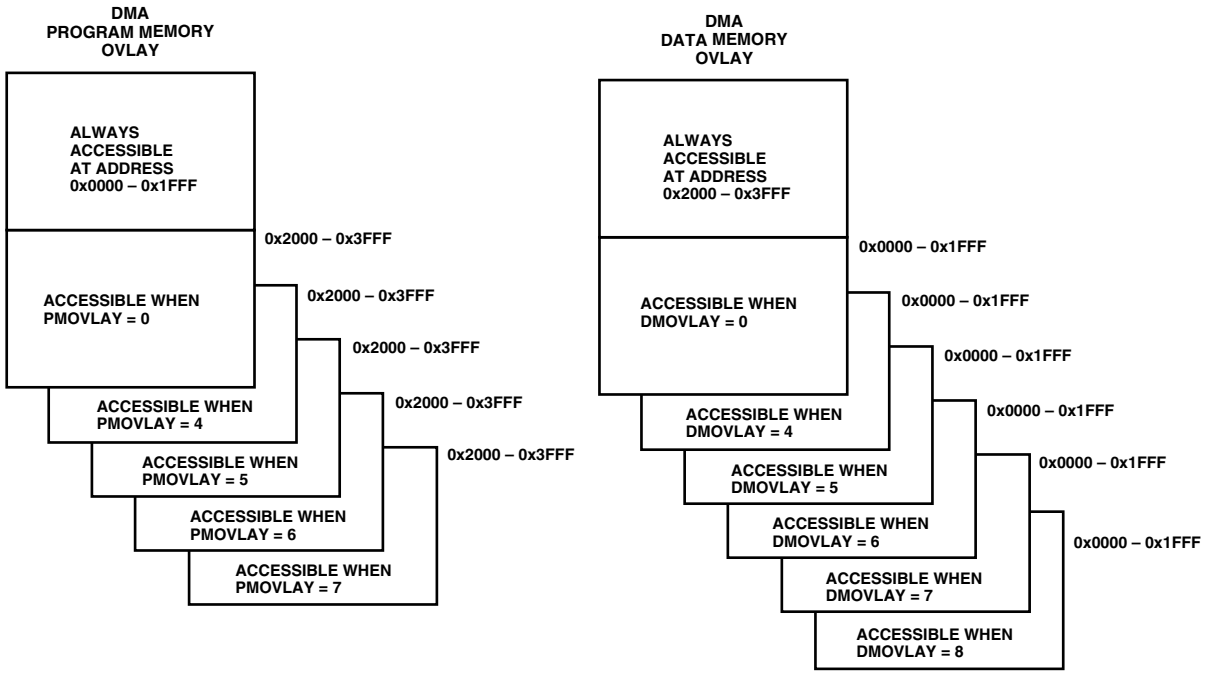


Figure 9. Direct Memory Access—PM and DM Memory Maps

IDMA Port Booting

The ADSP-21mod980 boots programs through its Internal DMA port. When Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-21mod980 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Flag I/O Pins

Each modem processor has eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-21mod980's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

Note: Pins PF0, PF1, and PF2 are also used for device configuration during reset. Since they are multiplexed within the ADSP-21mod980, PF[0:2] should be configured as an output for only one processor at a time.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-21mod980 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation, without replacing the target system processor, by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

The EZ-ICE can emulate only one modem processor at a time. You must include hardware to select which processor in the ADSP-21mod980 you want to emulate. Figure 10 is a functional representation of the modem processor selection hardware. One ICE-Port connector can be used with two ADSP-21mod980 processors without using additional buffers.

Issuing the "chip reset" command during emulation causes the modem processor to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly *prior* to issuing a chip reset command from the emulator user interface. As the mode pins share functionality with PF0:2 on the ADSP-21mod980, it may be necessary to reset the target hardware separately to ensure the proper mode selection state on emulator chip reset. See the *ADSP-2100 Family EZ-Tools* data sheet for complete information on ICE products.

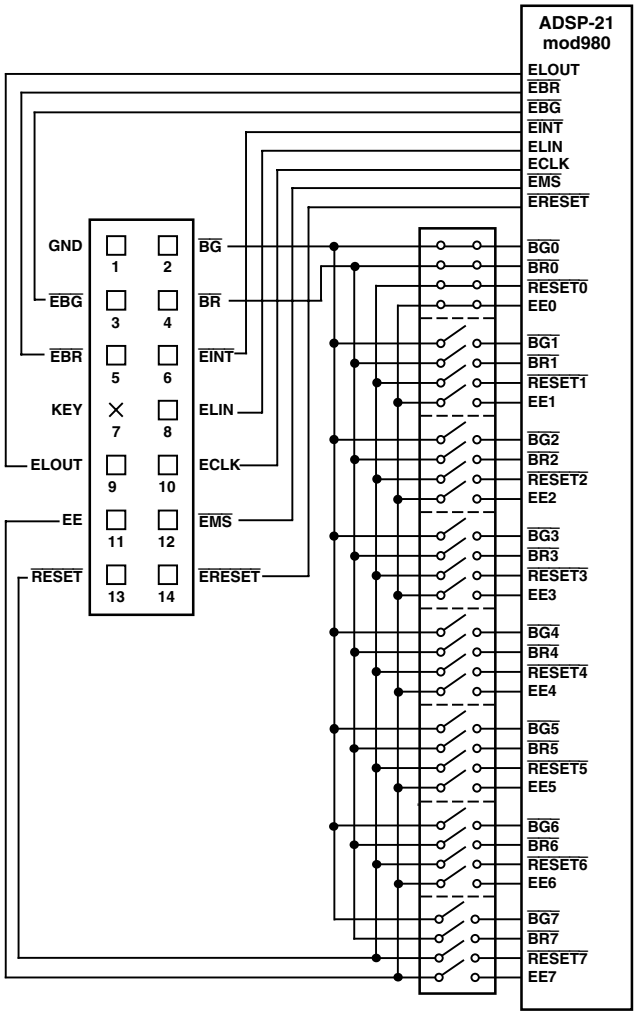


Figure 10. Selecting a Modem Processor in the ADSP-21mod980

The ICE-Port interface consists of the following ADSP-21mod980 pins:

$\overline{\text{EBR}}$	$\overline{\text{EMS}}$	ELIN
$\overline{\text{EBG}}$	$\overline{\text{EINT}}$	ELOUT
$\overline{\text{ERESET}}$	ECLK	EE

These ADSP-21mod980 pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-21mod980 and the connector must be kept as short as possible, no longer that 3 inches.

The following pins are also used by the EZ-ICE:

$\overline{\text{BR}}$ $\overline{\text{RESET}}$
$\overline{\text{BG}}$ GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-21mod980 in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in a system.

The EZ-ICE connects to the target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 10. This connector must be added to the target board design in order to use the EZ-ICE. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

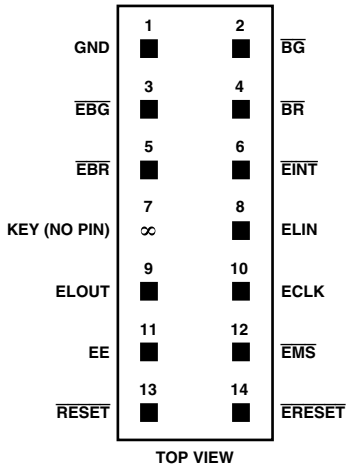


Figure 11. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For a target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between target circuitry and the processor on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between target circuitry and the processor on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (processor halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the processor's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's processor.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Max	Unit
V_{DDEXT}	2.97	3.63	V
V_{DDINT}	2.61	2.89	V
T_{AMB}	0	70	°C

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}, Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}, Hi-Level CLKIN Voltage	@ V_{DDINT} = max	2.0			V
V_{IL}, Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.7	V
V_{OH}, Hi-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.0			V
	@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
	@ V_{DDEXT} = min, V_{DDEXT} – 0.3 I_{OH} = –100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}, Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}, Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}, Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}, Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}, Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}, Supply Current (Idle)[9]	@ V_{DDINT} = 2.75, t_{CK} = 13.3 ns		80		mA
I_{DD}, Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.75, t_{CK} = 13.3 ns[11], T_{AMB} = 25°C		373		mA
I_{DD}, Supply Current (Power-Down)[12]	Lowest Power Mode		200		mA
C_I, Input Pin Capacitance[1, 3, 6, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			64	pF
C_O, Output Pin Capacitance[1, 6, 7, 12, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			64	pF

NOTES
[1]Bidirectional pins: RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, IAD [15:0], PF[2:0], PF[7:4].
[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{IS}}$, IAL, $\overline{\text{IRD}}$, $\overline{\text{IWR}}$.
[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1.
[4]Output pins: $\overline{\text{BG}}$, A0, DT0, DT1, CLKOUT, $\overline{\text{IACK}}$.
[5]Although specified for TTL outputs, all ADSP-21mod980 outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]Three-statable pins: DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, IAD[15:0], RFS1.
[8]0 V son $\overline{\text{BR}}$.
[9]Applies to PBGA package type.
[10]Output pin capacitance is the capacitive load for any three-stated output pin.
[11]V_{IN} = 0 V and 3 V. For typical supply current figures refer to Power Dissipation section.
[12]See the *ADSP-2100 Family User's Manual* for details.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max
Internal Supply Voltage (V_{DDINT})	–0.3 V	+3.0 V
External Supply Voltage (V_{DDEXT})	–0.3 V	+4.6 V
Input Voltage[1]	–0.5 V	+4.6 V
Output Voltage Swing[2]	–0.5 V	V_{DDEXT} + 0.5 V
Storage Temperature Range	–65 °C	+150 °C

NOTES
[1]Applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1).
[2]Applies to Output pins ($\overline{\text{BG}}$, PWDACK, A0, DT0, DT1, CLKOUT).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21mod980 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, the user cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. The user has no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-21mod980 timing parameter.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-21mod980 uses an input clock with a frequency equal to half the instruction rate: a 37.5 MHz input clock (which is equivalent to 26.6 ns) yields a 13.3 ns processor cycle (equivalent to 75 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 5 ns = 0.5 (13.3 ns) – 5 ns = 1.67 ns

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

T_{AMB} = T_{CASE} – (PD × θ_{JA})
T_J = Junction Temperature in °C
PD = Power Dissipation in W
θ_{JA} = Thermal Resistance (Junction-to-Ambient)

Package	θ_{JA}	Airflow
PBGA	28.2°C/W	0 lfm

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- Data memory is accessed every fourth cycle with 50% of the address pins switching.
- Data memory writes occur every fourth cycle with 50% of the data pins switching.
- Each address and data pin has a 64 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 13.3 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

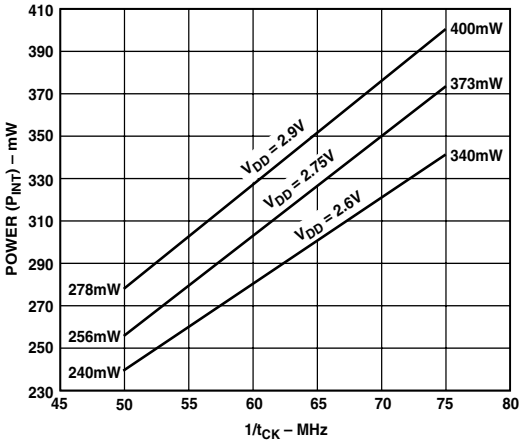
P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 12).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Table V. Example of Calculating Power Dissipation

	# of Pins	× C	× V_{DD}^2	×f
Address, $\overline{DMS}$	8	× 64 pF	× 3.3^2 V	18.8 MHz = 104.9 mW
Data Output, $\overline{WR}$	9	× 64 pF	× 3.3^2 V	18.8 MHz = 117.9 mW
				222.8 mW

Total power dissipation for this example is P_{INT} + 222.8 mW.



VALID FOR ALL TEMPERATURE GRADES
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 25°C
3. I_{DD} MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1,4,5,12,13,14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.

Figure 12. Power vs. Frequency

CAPACITIVE LOADING

Figures 13 and 14 show the capacitive loading characteristics of the ADSP-21mod980.

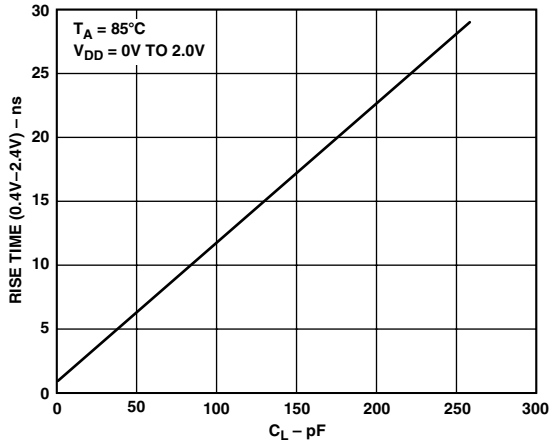


Figure 13. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

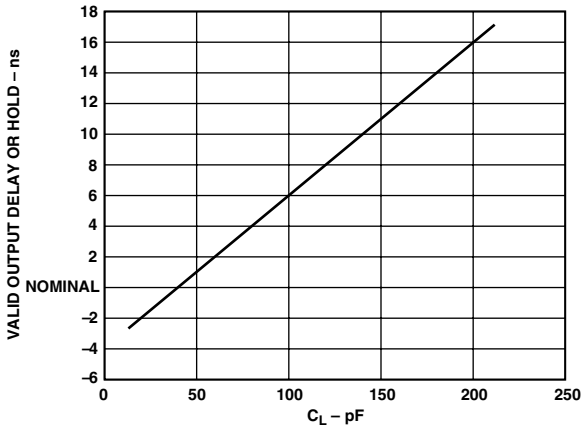


Figure 14. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 16. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

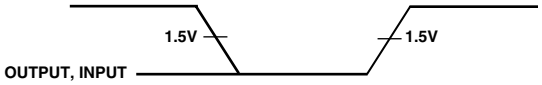


Figure 15. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, see Figure 16. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

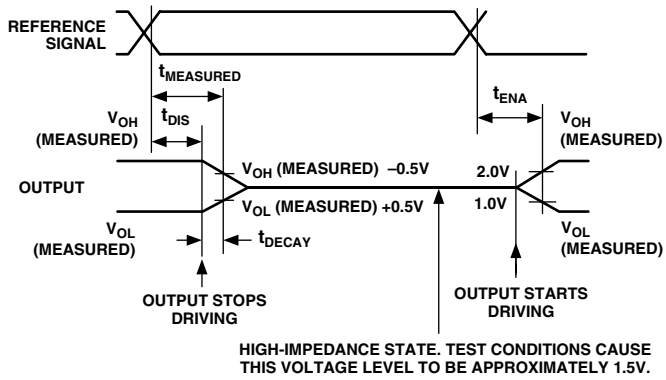


Figure 16. Output Enable/Disable

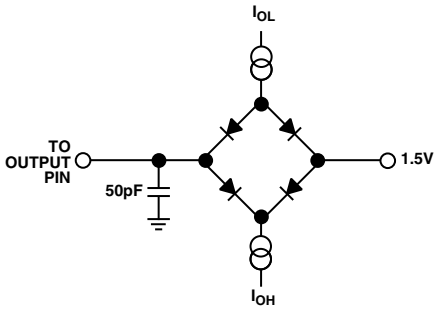


Figure 17. Equivalent Device Loading for AC Measurements (Including All Fixtures)

TIMING PARAMETERS

Parameter		75 MHz Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN Period	26.6	80	ns
t_{CKIL}	CLKIN Width Low	8		ns
t_{CKIH}	CLKIN Width High	8		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	0.5 t_{CK} – 2		ns
t_{CKH}	CLKOUT Width High	0.5 t_{CK} – 2		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	13	ns
Control Signals				
Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	5 t_{CK}[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Setup after $\overline{\text{RESET}}$ High	5		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

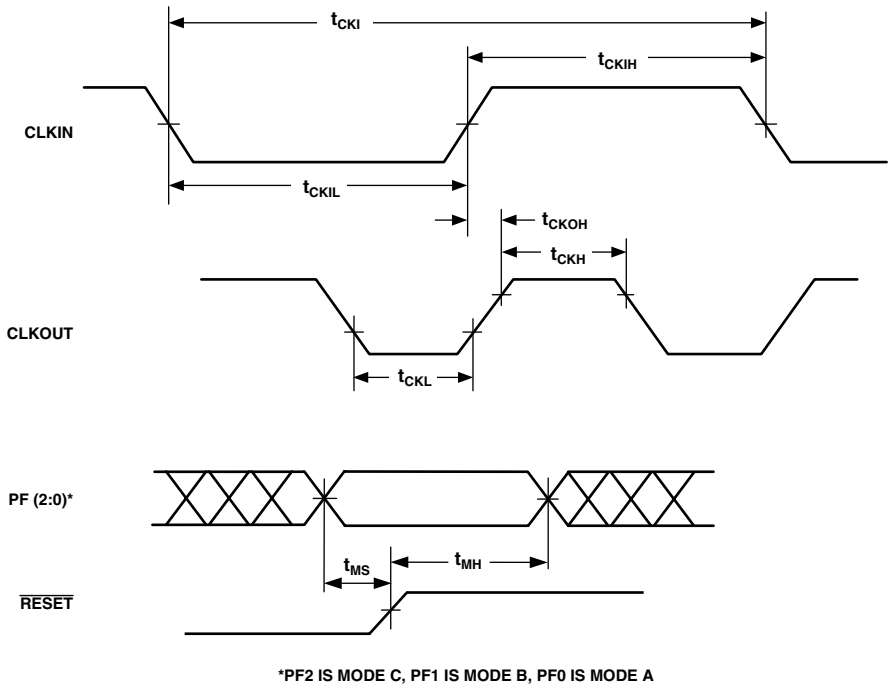


Figure 18. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	0.25 t_{CK} + 10		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	0.25 t_{CK}		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	0.25 t_{CK} – 5		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		0.5 t_{CK} + 4	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to Interrupt Controller Operation in the Program Control chapter of the *ADSP-2100 Family User's Manual*, Third Edition, for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$.
[4]PFx = PF0, PF1, PF2, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, Flag_out[4].

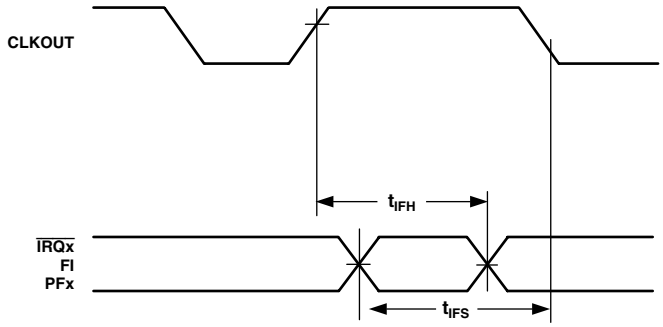


Figure 19. Interrupts and Flags

TIMING PARAMETERS

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	26.67		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	0.25 t_{CK}	0.25 t_{CK} + 6	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		12	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		12	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		12	ns
t_{SCDD}	SCLK High to DT Disable		12	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		12	ns

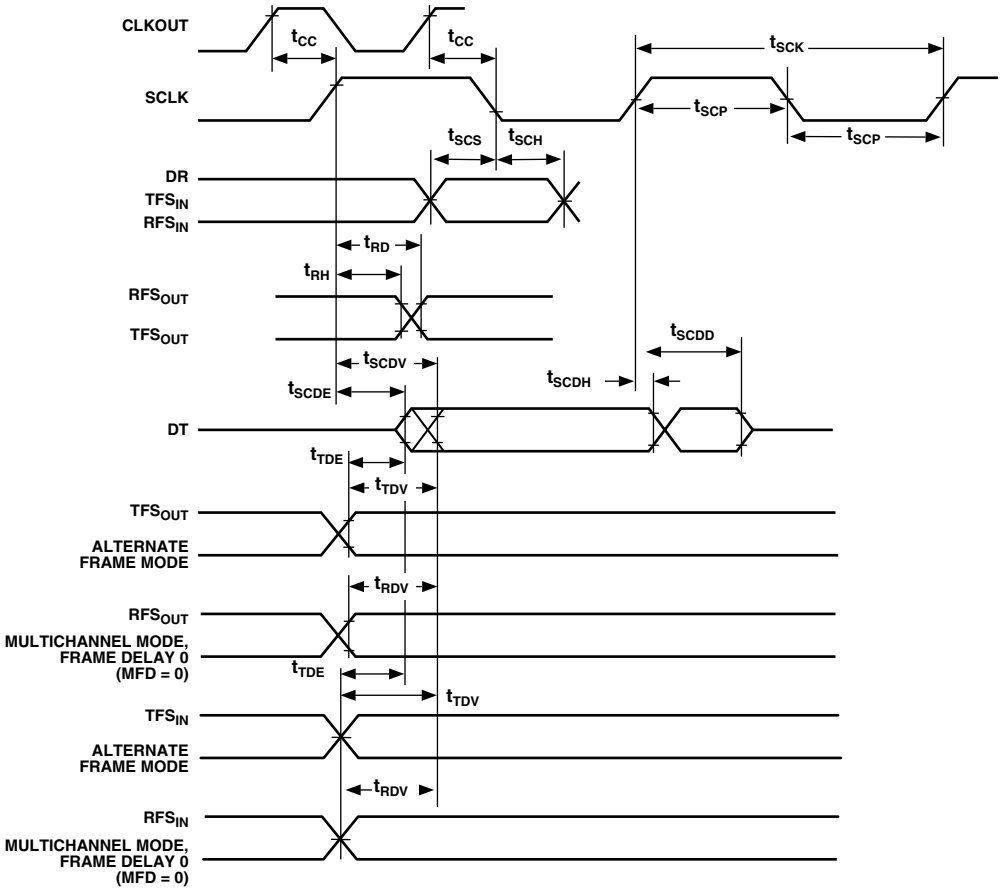


Figure 20. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	2		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[1, 2]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

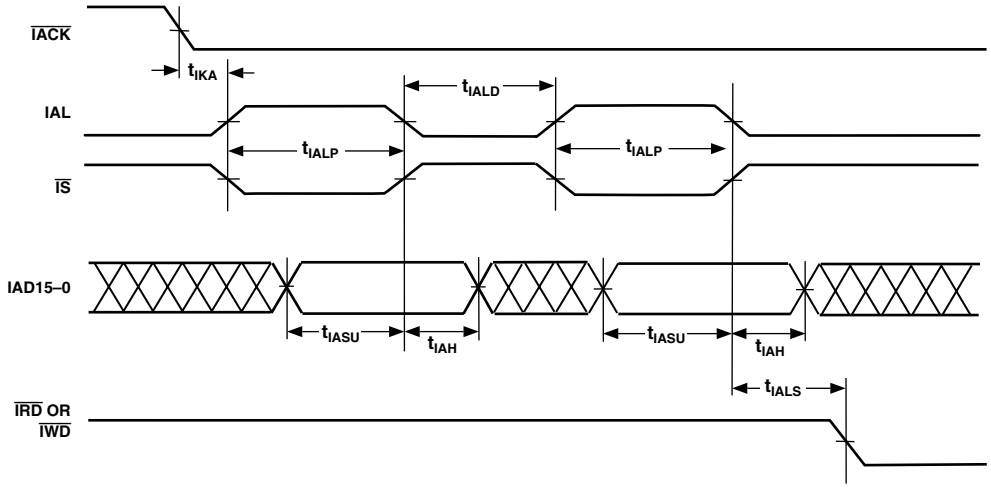


Figure 21. IDMA Address Latch

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

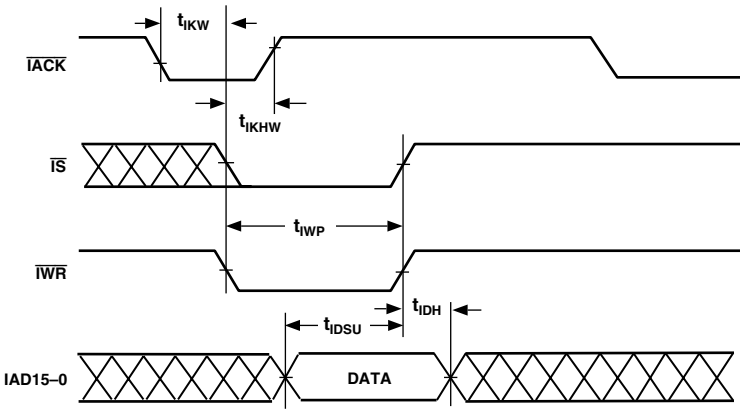


Figure 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	0.5 t_{CK} + 5		ns
t_{IKH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	1.5 t_{CK}		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual,* Third Edition.

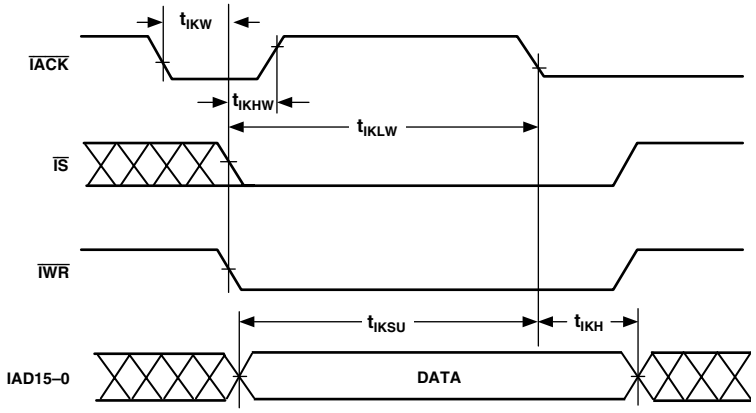


Figure 23. IDMA Write, Long Write Cycle

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	0.5 t_{CK} – 2		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	2 t_{CK} – 5		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	t_{CK} – 5		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

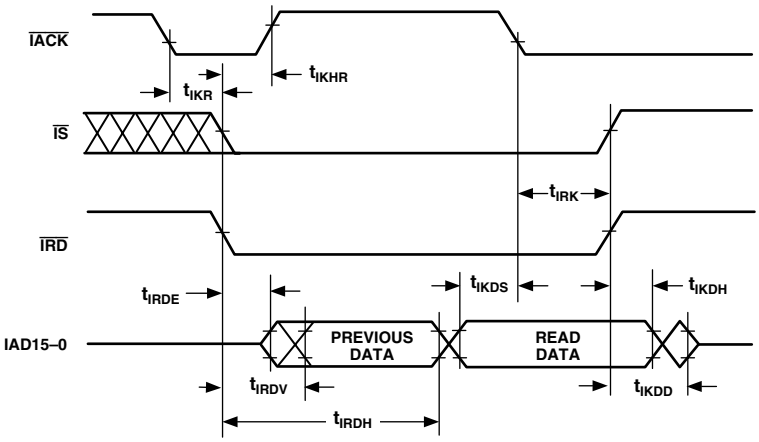


Figure 24. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle[1]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[4]	$2t_{CK}$ –5		ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (PM2)[5]	t_{CK} –5		ns

NOTES
[1]Timing applies to ADSP-21mod980 when Short Read only is disabled. See next page.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[4]DM read or first half of PM read.
[5]Second half of PM read.

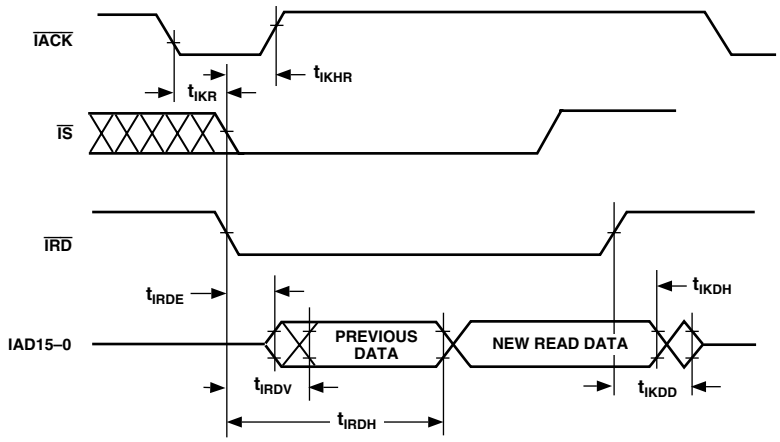


Figure 25. IDMA Read, Short Read Cycle

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle in Short Read Only Mode[1]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[1]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

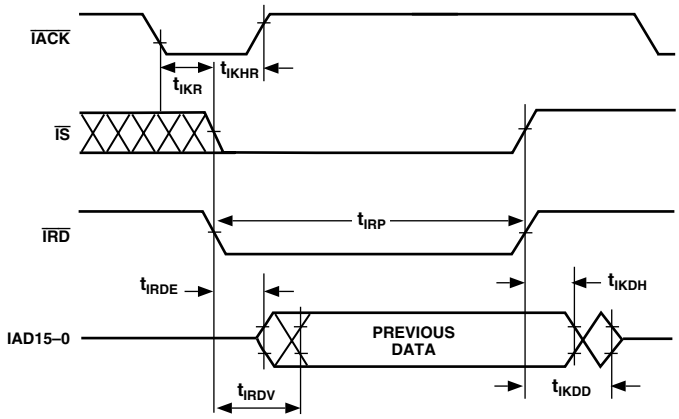


Figure 26. IDMA Read, Short Read Cycle

Pinout—Top View Left

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	A0	V_{DDINT}	V_{DDINT}	GND	PF0	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	CLKOUT_2	GND	DT1_2	V_{DDEXT}
B	IAD1_A	GND	V_{DDINT}	IAD0_A	GND	PF1	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	PF6_2	GND	GND	$\overline{BR\_2}$
C	IAD4_A	IAD2_A	GND	$\overline{IRD\_A}$	GND	PF2	V_{DDEXT}	IAL_A	V_{DDEXT}	PF4_2	GND	TFS0_2	EE_2
D	IAD14_A	IAD5_A	IAD3_A	GND	GND	$\overline{IS\_1}$	V_{DDEXT}	$\overline{IWR\_A}$	V_{DDEXT}	PF5_2	GND	PF7_2	$\overline{RESET\_2}$
E	DR0A	IAD13_A	CLKIN	IAD15_A									
F	GND	GND	$\overline{BG\_1}$	GND									
G	CLKOUT_1	GND	GND	$\overline{BR\_1}$									
H	GND	GND	GND	GND									
J	$\overline{RESET\_1}$	TFS0_1	RFS0A	PF7_1									
K	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}									
L	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}									
M	PF4_1	PF5_1	PF6_1	EE_1									
N	GND	GND	GND	GND									
P	SCLK0A	DT0A	DT1_1	CLKOUT_6									
R	V_{DDINT}	V_{DDINT}	V_{DDINT}	$\overline{BG\_6}$									
T	PF4_6	PF6_6	GND	$\overline{IACK\_A}$									
U	GND	GND	DT1_6	$\overline{BR\_6}$									
V	PF5_6	PF7_6	IAD11_A	IAD6_A									
W	GND	GND	GND	GND									
Y	TFS0_6	EE_6	IAD9_A	IAD7_A									
AA	$\overline{RESET\_6}$	IAD10_A	$\overline{IS\_4}$	IAD12_A									
AB	V_{DDINT}	V_{DDINT}	V_{DDINT}	V_{DDINT}									
AC	CLKOUT_4	PF4_4	PF5_4	GND	$\overline{BG\_4}$	GND	$\overline{IS\_6}$	GND	$\overline{BR\_4}$	GND	$\overline{RESET\_7}$	GND	EE_7
AD	PF6_4	GND	GND	GND	GND	IAD8_A	GND	GND	PF6_7	CLKOUT_7	GND	GND	DT1_7
AE	GND	GND	PF7_4	GND	TFS0_4	RFS1	DR1	GND	EE_4	GND	PF5_7	GND	V_{DDINT}
AF	GND	DT1_4	TFS1	GND	SCLK1	$\overline{RESET\_4}$	PF4_7	GND	PF7_7	GND	TFS0_7	GND	V_{DDINT}
	1	2	3	4	5	6	7	8	9	10	11	12	13

Pinout—Top View Right

14	15	16	17	18	19	20	21	22	23	24	25	26	
$\overline{IS\_2}$	V_{DDEXT}	GND	V_{DDEXT}	PF7_3	GND	GND	GND	D23	D22	D21	D18	GND	**A**
V_{DDEXT}	V_{DDEXT}	GND	V_{DDEXT}	PF6_3	GND	TFS0_3	GND	V_{DDEXT}	D19	D17	GND	D16	**B**
V_{DDEXT}	V_{DDEXT}	GND	V_{DDEXT}	PF5_3	GND	CLKOUT_3	GND	$\overline{RESET\_3}$	D20	GND	D15	D14	**C**
$\overline{BG\_2}$	V_{DDEXT}	GND	V_{DDEXT}	PF4_3	GND	GND	DT1_3	V_{DDEXT}	GND	D13	D12	D11	**D**
									$\overline{EMS}$	D10	D09	$\overline{ERESET}$	**E**
									D08	$\overline{IS\_3}$	$\overline{BG\_3}$	$\overline{EBG}$	**F**
									EE_3	PF5_5	$\overline{BR\_3}$	$\overline{EBR}$	**G**
									GND	GND	GND	GND	**H**
									ECLK	ELOUT	ELIN	$\overline{EINT}$	**J**
									V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	V_{DDEXT}	**K**
									IAD11_B	CLKOUT_5	PF4_5	IAD10_B	**L**
									IAD8_B	IAD9_B	IAD12_B	IAD6_B	**M**
									TFS0_5	$\overline{BR\_5}$	PF7_5	IAD7_B	**N**
									V_{DDINT}	V_{DDINT}	V_{DDINT}	V_{DDINT}	**P**
									GND	GND	$\overline{BG\_5}$	PF6_5	**R**
									$\overline{RESET\_5}$	GND	DT1_5	EE_5	**T**
									GND	GND	GND	GND	**U**
									IAD1_B	IAD2_B	$\overline{IS\_5}$	IAD0_B	**V**
									GND	IAD3_B	IAD4_B	IAD5_B	**W**
									$\overline{IWR\_B}$	$\overline{IRD\_B}$	IAL_B	$\overline{IS\_8}$	**Y**
									GND	GND	GND	GND	**AA**
									V_{DDINT}	V_{DDINT}	V_{DDINT}	V_{DDINT}	**AB**
V_{DDEXT}	V_{DDEXT}	$\overline{IS\text{-}7}$	GND	PF6_8	V_{DDEXT}	TFS0_8	GND	$\overline{RESET\_8}$	GND	IAD14_B	IAD15_B	$\overline{IACK\_B}$	**AC**
V_{DDEXT}	$\overline{BG\_7}$	GND	GND	PF4_8	V_{DDEXT}	RFS0B	GND	GND	GND	GND	$\overline{BG\_8}$	IAD13_B	**AD**
V_{DDEXT}	$\overline{BR\_7}$	GND	GND	PF5_8	V_{DDEXT}	DT1_8	GND	EE_8	GND	SCLK0B	GND	$\overline{BR\_8}$	**AE**
V_{DDEXT}	CLKOUT_8	GND	GND	PF7_8	V_{DDEXT}	DT0B	GND	DR0B	GND	V_{DDINT}	V_{DDINT}	GND	**AF**
14	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	

ADSP-21mod980

The ADSP-21mod980 package pinout is shown in the table below.

352-Ball PBGA Package Pinout

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
A0	A2	D11	D26	EE_1	M4	GND	AC12	GND	AF1
$\overline{BG\_1}$	F3	D12	D25	EE_2	C13	GND	AC17	GND	AF4
$\overline{BG\_2}$	D14	D13	D24	EE_3	G23	GND	AC21	GND	AF8
$\overline{BG\_3}$	F25	D14	C26	EE_4	AE9	GND	AC23	GND	AF10
$\overline{BG\_4}$	AC5	D15	C25	EE_5	T26	GND	AD2	GND	AF12
$\overline{BG\_5}$	R25	D16	B26	EE_6	Y2	GND	AD3	GND	AF16
$\overline{BG\_6}$	R4	D17	B24	EE_7	AC13	GND	AD4	GND	AF17
$\overline{BG\_7}$	AD15	D18	A25	EE_8	AE22	GND	AD5	GND	AF21
$\overline{BG\_8}$	AD25	D19	B23	$\overline{EINT}$	J26	GND	AD7	GND	AF23
$\overline{BR\_1}$	G4	D20	C23	ELIN	J25	GND	AD8	GND	AF26
$\overline{BR\_2}$	B13	D21	A24	ELOUT	J24	GND	AD11	GND	B2
$\overline{BR\_3}$	G25	D22	A23	$\overline{EMS}$	E23	GND	AD12	GND	B5
$\overline{BR\_4}$	AC9	D23	A22	ERESET	E26	GND	AD16	GND	B11
$\overline{BR\_5}$	N24	DR0A	E1	GND	A1	GND	AD17	GND	B12
$\overline{BR\_6}$	U4	DR0B	AF22	GND	A5	GND	AD21	GND	B16
$\overline{BR\_7}$	AE15	DR1	AE7	GND	A11	GND	AD22	GND	B19
$\overline{BR\_8}$	AE26	DT0A	P2	GND	A16	GND	AD23	GND	B21
CLKIN	E3	DT0B	AF20	GND	A19	GND	AD24	GND	B25
CLKOUT1	G1	DT1_1	P3	GND	A20	GND	AE1	GND	C3
CLKOUT_2	A10	DT1_2	A12	GND	A21	GND	AE2	GND	C5
CLKOUT_3	C20	DT1_3	D21	GND	A26	GND	AE4	GND	C11
CLKOUT_4	AC1	DT1_4	AF2	GND	AA23	GND	AE8	GND	C16
CLKOUT_5	L24	DT1_5	T25	GND	AA24	GND	AE10	GND	C19
CLKOUT_6	P4	DT1_6	U3	GND	AA25	GND	AE12	GND	C21
CLKOUT_7	AD10	DT1_7	AD13	GND	AA26	GND	AE16	GND	C24
CLKOUT_8	AF15	DT1_8	AE20	GND	AC4	GND	AE17	GND	D4
D08	F23	$\overline{EBG}$	F26	GND	AC6	GND	AE21	GND	D5
D09	E25	$\overline{EBR}$	G26	GND	AC8	GND	AE23	GND	D11
D10	E24	ECLK	J23	GND	AC10	GND	AE25	GND	D16

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
GND	D19	GND	W23	IAD8_B	M23	PF5_5	G24	SCLK0B	AE24
GND	D20	$\overline{\text{IACK\_A}}$	T4	IAD9_A	Y3	PF5_6	V1	SCLK1	AF5
GND	D23	$\overline{\text{IACK\_B}}$	AC26	IAD9_B	M24	PF5_7	AE11	TFS0_1	J2
GND	F1	IAD0_A	B4	IAL_A	C8	PF5-8	AE18	TFS0_2	C12
GND	F2	IAD0_B	V26	IAL_B	Y25	PF6_1	M3	TFS0_3	B20
GND	F4	IAD1_A	B1	$\overline{\text{IRD\_A}}$	C4	PF6_2	B10	TFS0_4	AE5
GND	G2	IAD1_B	V23	$\overline{\text{IRD\_B}}$	Y24	PF6_3	B18	TFS0_5	N23
GND	G3	IAD10_A	AA2	$\overline{\text{IS\_1}}$	D6	PF6_4	AD1	TFS0_6	Y1
GND	H1	IAD10_B	L26	$\overline{\text{IS\_2}}$	A14	PF6_5	R26	TFS0_7	AF11
GND	H2	IAD11_A	V3	$\overline{\text{IS\_3}}$	F24	PF6_6	T2	TFS0_8	AC20
GND	H3	IAD11_B	L23	$\overline{\text{IS\_4}}$	AA3	PF6_7	AD9	TFS1	AF3
GND	H4	IAD12_A	AA4	$\overline{\text{IS\_5}}$	V25	PF6_8	AC18	V_{DDEXT}	A7
GND	H23	IAD12_B	M25	$\overline{\text{IS\_6}}$	AC7	PF7_1	J4	V_{DDEXT}	A8
GND	H24	IAD13_A	E2	$\overline{\text{IS\_7}}$	AC16	PF7_2	D12	V_{DDEXT}	A9
GND	H25	IAD13_B	AD26	$\overline{\text{IS\_8}}$	Y26	PF7_3	A18	V_{DDEXT}	A13
GND	H26	IAD14_A	D1	$\overline{\text{IWR\_A}}$	D8	PF7_4	AE3	V_{DDEXT}	A15
GND	N1	IAD14_B	AC24	$\overline{\text{IWR\_B}}$	Y23	PF7_5	N25	V_{DDEXT}	A17
GND	N2	IAD15_A	E4	PF0	A6	PF7_6	V2	V_{DDEXT}	AC14
GND	N3	IAD15_B	AC25	PF1	B6	PF7_7	AF9	V_{DDEXT}	AC15
GND	N4	IAD2_A	C2	PF2	C6	PF7_8	AF18	V_{DDEXT}	AC19
GND	R23	IAD2_B	V24	PF4_1	M1	$\overline{\text{RESET\_1}}$	J1	V_{DDEXT}	AD14
GND	R24	IAD3_A	D3	PF4_2	C10	$\overline{\text{RESET\_2}}$	D13	V_{DDEXT}	AD19
GND	T3	IAD3_B	W24	PF4_3	D18	$\overline{\text{RESET\_3}}$	C22	V_{DDEXT}	AE14
GND	T24	IAD4_A	C1	PF4_4	AC2	$\overline{\text{RESET\_4}}$	AF6	V_{DDEXT}	AE19
GND	U1	IAD4_B	W25	PF4_5	L25	$\overline{\text{RESET\_5}}$	T23	V_{DDEXT}	AF14
GND	U2	IAD5_A	D2	PF4_6	T1	$\overline{\text{RESET\_6}}$	AA1	V_{DDEXT}	AF19
GND	U23	IAD5_B	W26	PF4_7	AF7	$\overline{\text{RESET\_7}}$	AC11	V_{DDEXT}	B7
GND	U24	IAD6_A	V4	PF4_8	AD18	$\overline{\text{RESET\_8}}$	AC22	V_{DDEXT}	B8
GND	U25	IAD6_B	M26	PF5_1	M2	RFS0A	J3	V_{DDEXT}	B9
GND	U26	IAD7_A	Y4	PF5_2	D10	RFS0B	AD20	V_{DDEXT}	B14
GND	W1	IAD7_B	N26	PF5_3	C18	RFS1	AE6	V_{DDEXT}	B15
GND	W2	IAD8_A	AD6	PF5_4	AC3	SCLK0A	P1	V_{DDEXT}	B17
GND	W3								
GND	W4								

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
V_{DDEXT}	B22	V_{DDEXT}	D17	V_{DDEXT}	K26	V_{DDINT}	AB3	V_{DDINT}	AF25
V_{DDEXT}	C7	V_{DDEXT}	D22	V_{DDEXT}	L1	V_{DDINT}	AB4	V_{DDINT}	B3
V_{DDEXT}	C9	V_{DDEXT}	K1	V_{DDEXT}	L2	V_{DDINT}	AB23	V_{DDINT}	P23
V_{DDEXT}	C14	V_{DDEXT}	K2	V_{DDEXT}	L3	V_{DDINT}	AB24	V_{DDINT}	P24
V_{DDEXT}	C15	V_{DDEXT}	K3	V_{DDEXT}	L4	V_{DDINT}	AB25	V_{DDINT}	P25
V_{DDEXT}	C17	V_{DDEXT}	K4	V_{DDINT}	A3	V_{DDINT}	AB26	V_{DDINT}	P26
V_{DDEXT}	D7	V_{DDEXT}	K23	V_{DDINT}	A4	V_{DDINT}	AE13	V_{DDINT}	R1
V_{DDEXT}	D9	V_{DDEXT}	K24	V_{DDINT}	AB1	V_{DDINT}	AF13	V_{DDINT}	R2
V_{DDEXT}	D15	V_{DDEXT}	K25	V_{DDINT}	AB2	V_{DDINT}	AF24	V_{DDINT}	R3

ORDERING GUIDE

Part Number	Ambient Temperature Range	Processor Clock	Package Description	Package Option
ADSP-21mod980-000	0°C to 70°C	37.5 MHz	Plastic Ball Grid Array (PBGA)	B-352

RELATED DOCUMENTS

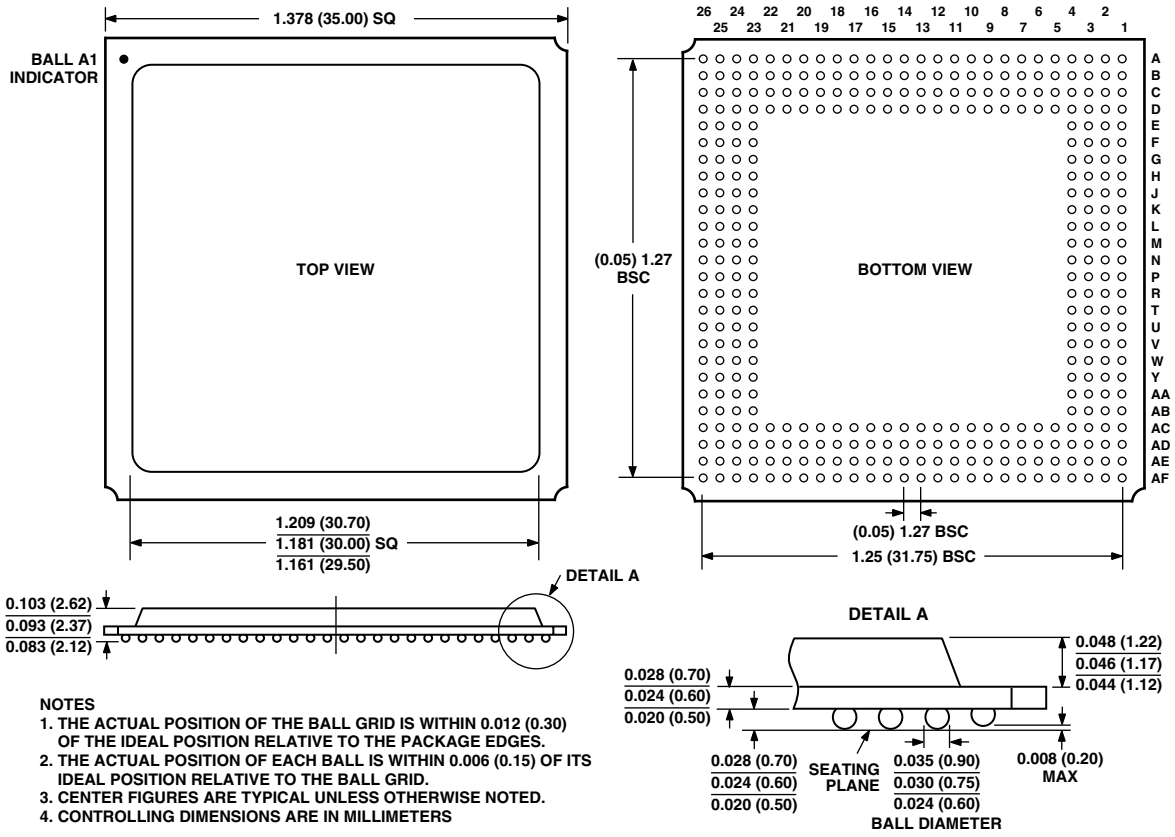
ADSP-21mod980-210 Multiport Internet Gateway Processor Solution.
ADSP-21mod Family Dynamic Internet Voice Access™ (DIVA) Voice Over Network Solution.

DIVA is a trademark of Analog Devices, Inc.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

352-Ball Grid Array (PBGA)
(B-352)



NOTES
1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.012 (0.30) OF THE IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.006 (0.15) OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
3. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
4. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

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