AN6448NFBP

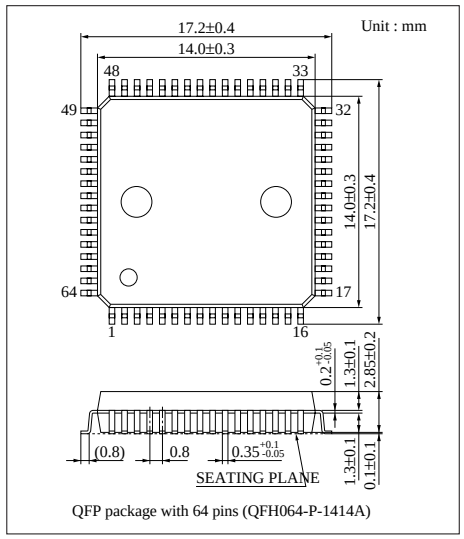
Speech Network IC Incorporating Cross-Point Switch

■ Overview

The AN6448NFBP is a speech network IC suitable for multi-function cordless telephones. It incorporates a cross-point switch controlled by serial input. It allows speech path switching and mixing, and provides for three- or four-person communication and other sophisticated functions. It also incorporates REC/PLAY amplifiers with VOX circuits.

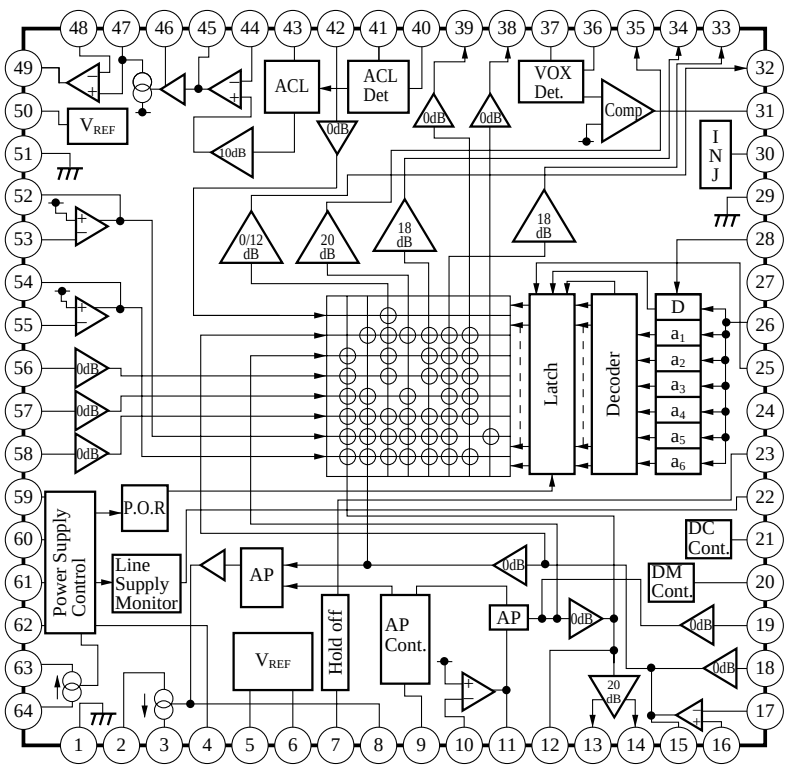
■ Features

- The speech block can operate on line voltage, with no external power supply, and is operational even during a commercial power failure.
- Incorporates auto. PAD, dial mute, DC voltage regulation, and other basic speech functions.
- The cross-point switch can be operated independently.
- Each output of the cross-point switch can correspond to multiple inputs, allowing three-or four-person communication.
- The REC/PLAY amplifiers incorporate ALC and VOX circuits.
- Receiver volume can be increased by 6 dB or 9 dB.



QFP package with 64 pins (QFH064-P-1414A)

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	7.0	V
Supply current (1)	I_{CC}	50	mA
Supply voltage (2)	V_L	12.0	V
Supply current (2)	I_L	135	mA
Power dissipation Note)	P_D	640	mW
Operating ambient temperature	T_{opr}	–20 to +75	˚C
Storage temperature	T_{stg}	–55 to +150	˚C

Note) In a free-air condition with Ta=75˚C.

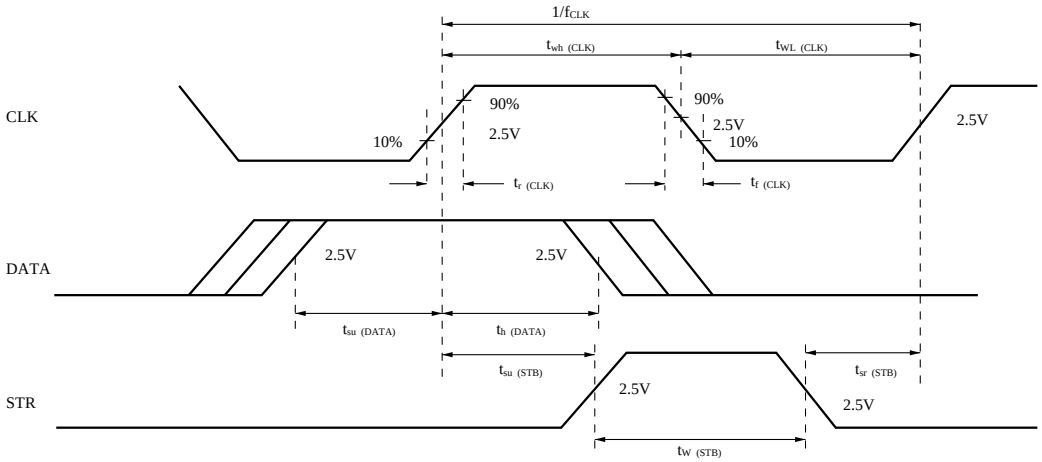
■ Recommended Operating Conditions (Ta=25˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Operating supply voltage range (1)	V_{CC}		4.5	5	5.5	V
Operating supply voltage range (2)	V_L		3	—	11	V
Clock frequency	f_{CLK}		—	—	250	kHz

■ Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Speech network block						
Rec. gain	G_V–ER1	I_L=30mA, V_{CC}=5V, Vin=–42dBm	30.5	32.5	34.5	dB
Rec. automatic PAD width	AP–ER	I_L=30 to 80mA, V_{CC}=5V, Vin=–42dBm	2.5	3.7	5	dB
Trans. gain	G_V–EM1	I_L=30mA, V_{CC}=5V, Vin=–38dBm	27.7	29.7	31.7	dB
Trans. automatic PAD width	AP–EM	I_L=30 to 80mA, V_{CC}=5V, Vin=–38dBm	2.5	4	5	dB
DTMF gain	G_V–ED1	I_L=30mA, V_{CC}=5V, DM=ON, Vin=–30dBm	16.9	18.9	20.9	dB
DTMF automatic PAD width	AP–EDT	I_L=30 to 80mA, V_{CC}=5V, V–DMC=LOW, Vin=–30dBm	2.5	4.1	5.5	dB
REC/PLAY amp. block						
Head bias current	I–REC		145	180	215	µA
REC preamp. output	V_O–RP	Vin=–45dBm, Rin=10kΩ	–13.4	–11.4	–9.4	dBm
EQ amp. gain	G_V–EQ	Vin=–40dBm	27.8	29.8	31.8	dB
Switch block						
SP out max output	V_O–SP	Input L-SP IN, THD=5%	0	4	—	dBm
DH out max output	V_O–DH	Input RF1 IN, THD=5%	0	4	—	dBm
RF1 out max output	V_O–RF1	Input RF2 IN, THD=5%	0	4	—	dBm
RF2 out max output	V_O–RF2	Input RF1 IN, THD=5%	0	4	—	dBm
L-REC out max output	V_O–LR	Input AUX IN, THD=5%	0	4	—	dBm

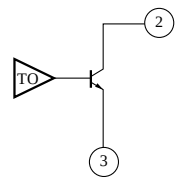
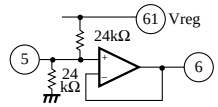
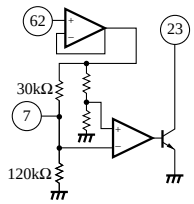
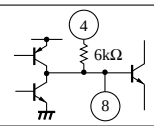
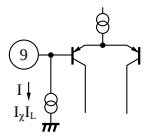
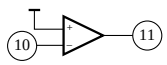
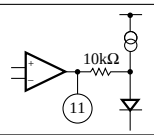
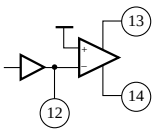
■ Timing Chart



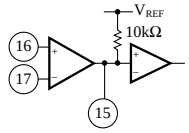
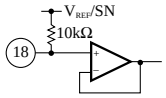
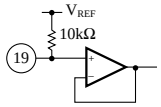
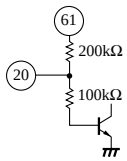
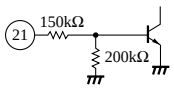
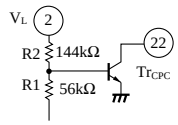
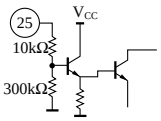
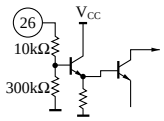
■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Ground	33	RF2 link output
2	Line power (+) input	34	RF1 link output
3	Side-tone adjustment	35	Intercom link output
4	Line voltage control (1)	36	VOX detection control
5	Int. ref. voltage output (1)	37	VOX amp. input
6	Int. ref. voltage output (2)	38	Time stamp link output
7	Hold-reset control	39	Recording link output
8	Trans. preamp. output	40	ALC input
9	Auto. PAD control	41	ALC detection control
10	Rec. preamp. input	42	Loudspeaker link input
11	Rec. preamp. output	43	Recording input
12	Rec. amp. input	44	Recording inverse input
13	Rec. amp. output (1)	45	Recording preamp. output
14	Rec. amp. output (2)	46	Recording bias current control
15	MIC preamp. output	47	To recording head
16	MIC preamp. input (1)	48	EQ amp. inverse input
17	MIC preamp. input (2)	49	EQ amp. output
18	DTMF signal input	50	REC/PLAY int. ref. voltage output
19	BT signal input	51	Ground
20	Dial mute control	52	MIX preamp. output
21	Line voltage control	53	MIX link input
22	Line interruption detector output	54	AUX preamp. output
23	Hold-reset signal output	55	AUX link input
24	No connection	56	Intercom link input
25	Strobe signal input	57	RF1 link input
26	Clock signal input	58	RF2 link input
27	No connection	59	Power-ON reset control
28	Data input	60	External supply voltage input
29	Ground	61	Internal supply voltage output
30	Logic power supply input	62	Circuit voltage control (2)
31	VOX detector output	63	Line current bypass (2)
32	SP link output	64	Line current bypass (1)

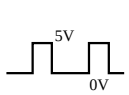
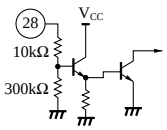
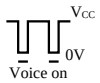
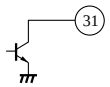
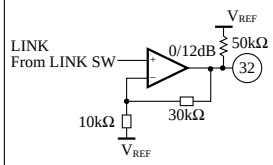
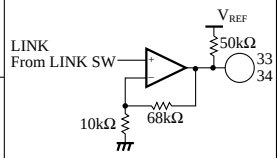
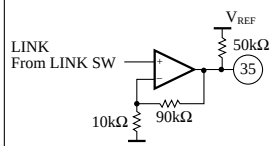
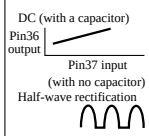
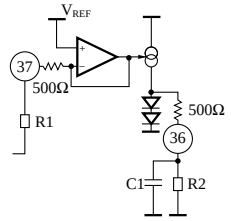
■ Pin Descriptions

PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
1	GND	—	0V	Ground : • This is the ground pin for the speech network.	GND for REC/PLY, VRER SPEECH and LINK.	
2	V_L	I	DC 3 to 10V	Line power input : • Connects to the positive output of the diode bridge.		The line drive gain (G) is : $G = \frac{Z_{Line} // Z_{Tel}}{R_1}$ Also assuming $Z_{Line} \simeq 600\Omega$ $Z_{Tel} \simeq 600\Omega$ $R_1 = 27\Omega$: $G = 20\log \frac{300}{27} = 20.9dB$
3	ST	O	DC 0.3V	Side-tone adjustment : • Grounded through R1 (27Ω). • Connects to the side-tone adjusting circuit to adjust side tone and receiver level.		
4	V_L– CONT	I	DC1V	Line voltage control (1) :		C_2 and the internal resistance determine the f. characteristics.
5	V_{REF}	O	1V (Const)	Int. ref. voltage output (1) : • Outputs half the Vreg reference voltage. • Grounded through a 0.01μF capacitor.		———
6	V_{REF}– SN	O	1V (Const)	Int. ref. voltage output (2) : • Output impedance=50Ω		
7	HCO	—	I_L	Hold-reset control : • Grounded through C5. Adjusts the output time of control signals.		The larger the capacitance of C_5, the wider the pulse width.
23	HCC	—	V_{CC} 0V Hold-reset signal	Hold-reset signal output : • This is an open-collector output to a microprocessor. • Requires a pull-up resistor.		
8	T– FILTER	O	DC1V	Trans. preamp. output : • C_6 as connected between this pin and the ground forms a low-pass filter.		C6 and the 6-kΩ internal resistance as illustrated on the left form a low-pass filter.
9	APC	I	Vreg-R · I I_L	Auto. PAD control : • Connects through a resistance to Pin61 (Vreg). If the resistance increases, the PAD operates closer to the near end. If the resistance decreases, the PAD operates closer to the far end.		———
10	RV IN	I	V_{REF}	Rec. preamp. input : • Receiver signals are input from the side-tone circuit to this pin. • R7 and C8 connected between Pin11 and this pin determine		The receiver preamplifier gain (G) is : $G = -20\log \left(\frac{1}{\frac{1}{R7} + \omega C8} \Big/ R6 + \frac{1}{\omega C9} \right)$
11	RV PRE– OUT	O	V_{REF}	Rec. preamp. output : • R7 and C8 connected between Pin10 and this pin determine the f. characteristics. • The output impedance is 100 ±50Ω.		
12	RV FILTER	O	V_{REF}	Rec. amp. input :		The larger the capacitance of C10, the lower the high band gain as with a LPF.
13 . 14	RV OUT (1) RV OUT (2)	O	V_{REF} V_{REF}	Rec. amp. outputs (1 and 2) : • A ceramic or dynamic receiver is connected. • The output circuit is a BTL configuration. • The output impedance is 50± 30Ω.		

■ Pin Descriptions (cont.)

PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
15	MIC OUT	O	V_{REF}	MIC preamp. output : • R11 and C13 connected between Pin17 and this pin determine the f. characteristics. • The output impedance is 300 ±100Ω.		Feedback is input to this pin through a capacitor. The capacitor and R9 to R11, and C12 and C13 determine the f. characteristics.
16	MIC IN (+)	I		MIC preamp. input (1) : • A bias resistor and a microphone connect to this pin.		
17	MIC IN (–)	I	V_{REF}	MIC preamp. input (2) : • R11 and C13 connected between Pin15 and this pin determine the f. characteristics.		
18	MF– IN	I	V_{REF} With signal ON	DTMF signal input : • DTMF signals are input through a coupling capacitor C14. • When DMC is low at Pin20, DTMF is enabled. • Input impedance is 10kΩ.		The input impedance (10kΩ) and C14 or C15 form an input HPF.
19	BT– IN	I	V_{REF} With signal ON	BT signal input : • Beep tone (BT) signals are input through a coupling capacitor C15. • Input impedance is 10kΩ.		
20	DMC	I		Dial mute control : • Normal speech mode when Pin20 is high or open (MIC amp. ON and rec. amp. ON). • DTMF mode when Pin20 is low (DTMF amp. ON and BT amp. ON).		———
21	DC– CONT	I	V_{CC} 0.2V Line voltage increases	Line voltage control : • Line voltage is normal when this pin is high. Line voltage increases by 1 to 1.5V when this pin is low.		———
22	CPC	O	V_{CC} 0.2V Line interruption	Line interruption detector output : • This is an open collector output to a microprocessor, requiring a pull-up resistor connected to the microprocessor's power supply. This pin goes low when line voltage is 3.0V or more, and goes high when 1.5V or less.		• Referring to the left figure, the voltage, VCPC, at which T_{rCPC} turns ON is calculated as follows: V_{CPC} (ON) $= \frac{R1+R2}{R1} \times VBE\ (T_{rCPC})$ = 2.5V (Ta=25˚C)
24	NC			No connection		
25	STR	I	5V 0V	Strobe signal input : • The strobe signal for serial control data is input to this pin. The rising edge of the strobe signal determines the timing at which internal control address or ON/OFF status is validated.		———
26	CLK	I	5V 0V	Clock signal input : • The clock signal for serial control data is input to this pin. The rising edge of the clock signal determines the timing at which data is read.		———
27	NC			No connection		

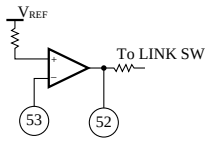
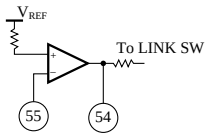
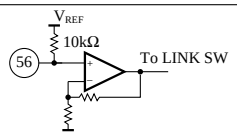
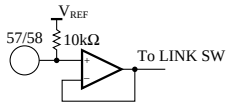
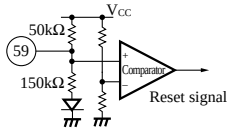
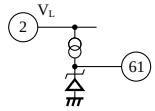
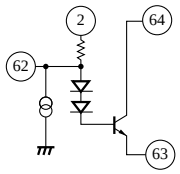
■ Pin Descriptions (cont.)

PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
28	DATA	I		Data input : • Serial data is input to this pin. Data is read into the internal shift register in synchronization with clock signals.		———
29	GND	—	—	Ground : • This is the ground pin for the logic circuits.		
30	L – V_{CC}	—	—	Logic power supply input :		
31	VOX. OUT	O		VOX detector output : • This is an open collector output. • This pin goes low when voice signals are input to Pin37.		• Output waveforms are shaped stable internally (by the threshold circuit).
32	SP. OUT	O		Loudspeaker link output : • This is a link switch output to an external loudspeaker amplifier. • The output amplifier gain is selectable between 12 and 0dB. • Output impedance is 50±30Ω.		When address 2F of the cross-point switch is OFF, the output amplifier gain is set to 12 dB.
33	RF2 – OUT	O		RF2 link output : • This is a link switch output. • Output impedance is 50±30Ω.		
34	RF1 – OUT	O		RF1 link output : • This is a link switch output. • Output impedance is 50±30Ω.		
35	DH – OUT	O		Intercom link output : • This is a link switch output to a intercom. • Output impedance is 50±30Ω.		
36	VOX DET	O		VOX detection control : • A smoothing capacitor (C17) and a resistor (R19) connect in parallel to this pin to adjust the attack and recovery times of the VOX detector.		• VOX detection can be done in two ways : A) With small C17 (560pF) and small R19 (39kΩ) VOX input VOX output B) With large C17 (22µF) and large R19 (100kΩ) VOX input VOX output • Input sensitivity is calculated as follows : $G = \frac{R2//ZC1}{R1}$ Adjust the f. characteristics and sensitivity based on the above calculation.
37	VOX IN	I		VOX amp. input : • VOX (voice detection) signals are input to this pin. • Input impedance is 500Ω.		

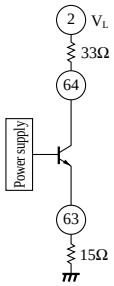
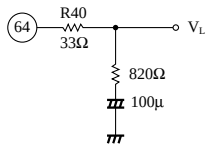
■ Pin Descriptions (cont.)

PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
38	LTS – OUT	O	V_{REF}	Time stamp link output : • This is a buffered link switch output. • Output impedance is 50±30Ω.	LINK To LINK SW 38 39	
39	LRC – OUT	O	V_{REF}	Recording link output : • This is a buffered link switch output. • Output impedance is 50±30Ω.		
40	ALC. IN	I		ALC input : • Pin45 connects through a coupling capacitor to this pin. • Input impedance is 10kΩ.	V_{CC} V_{REF} 40 2kΩ 41	• Ground Pin41 if no ALC circuit is used. • The larger C20, the longer the attack time. The smaller R22, the shorter the recovery time.
41	ALC. DET	O	DC (with a capacitor) Pin$1 output Input (with no capacitor) Full-wave rectification	ALC detection control : • A smoothing capacitor (C20) and a resistor (R22) connect in parallel to this pin to adjust the attack and recovery times of the ALC.		
42	SP – IN	I	V_{REF}	Loudspeaker link input : • SP signals to this pin are output through a coupling capacitor to the link switch. • Input impedance is 50kΩ.	V_{REF} LINK To LINK SW 42 50kΩ	———
43	RD PRE – IN	I	V_{REF}	Recording input : • Recording signals are input through a coupling capacitor to this pin. • Input impedance is normally 10 kΩ. It decreases during ALC operation.	V_{REF} 10kΩ 43 10kΩ 22kΩ From ALC	———
44	RD PRE – NF	I	V_{REF}	Recording preamp. inverse input : • A C/R combination between Pin45 and this pin determines the gain and f. characteristics of the recording preamplifier.	45 44	The gain (G) of the recording preamplifier is : $G = -\frac{R26}{R24 + \frac{1}{\omega C23}}$
45	REC PRE – OUT	O	V_{REF}	Recording preamp. output : • Outputs amplified recording signals. • Output impedance is 50±30Ω.		
46	BIAS ADJ	—	V_{REF}	Recording bias current control : • A C/R combination connected to this pin determines the recording bias current and gain of a recording head. • The smaller the resistance of the C/R combination, the greater the bias current and gain.	V_{CC} 61 45 46 R27 47	• Address 07 of the cross-point SW determines the ON/OFF status of the rec. preamp. • The bias current to the head is : $I_H = \frac{Vref}{R27} \times 3$ $V_{ref} = \frac{1}{2} V_{REG}$
47	HEAD	I/O	Bias voltage During recording 0V During playing 0V	To recording head : • A recording head connects to this pin.		
48	EQ. NF	I	V_{REF}	EQ amp. inverse input : • A C/R combination between pin49 and this pin determines the equalizer characteristics.	V_{REF} From recording head 49 48	• The gain of the equalizer amp. is calculated the same way as the receiver preamp. • Address 0F of the cross-point SW determines the ON/OFF status of the EQ amp.
49	EQ. OUT	O	V_{REF}	EQ amp. output : • Outputs amplified equalizer signals. • Output impedance is 50±30Ω.		
50	V_{REF} – PR	O	$\frac{1}{2}V_{REF}$ (CONST)	REC/PLAY int. ref. voltage output : • The pin5 ref. voltage is buffered and output from this pin.	V_{REF} 5 50	———

■ Pin Descriptions (cont.)

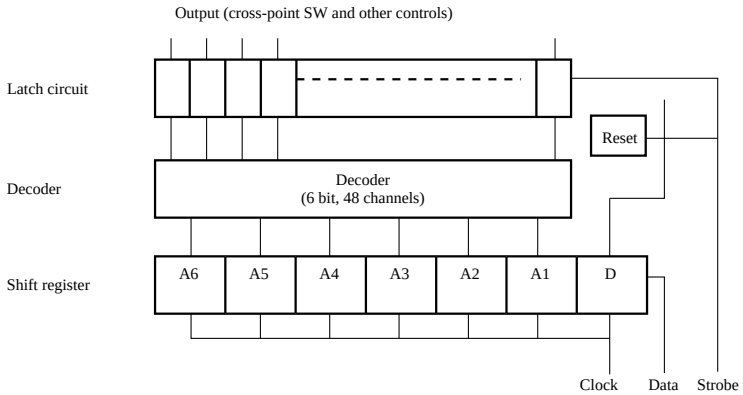
PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
51	GND	—	——	Ground : • Output impedance is 50±30Ω.	——	——
52	MIX OUT	O	V_{REF}	MIX preamp. output : • A C/R combination between Pin53 and this pin determines the gain and f. characteristics of the MIX pre-amp. • Output impedance is 50±30Ω.		The gain of the MIX preamp. is calculated the same way as the rec. preamp.
53	MIX IN	I	——	MIX link input : • MIX signals are input through a coupling capacitor to this pin.		
54	AUX OUT	O	V_{REF}	AUX preamp. output : • A C/R combination between Pin55 and this pin determines the gain and f. characteristics of the AUX pre-amp. • Output impedance is 50±30Ω.		The gain of the AUX preamp. is calculated the same way as the rec. preamp.
55	AUX IN	I	——	AUX link input : • AUX signals are input through a coupling capacitor to this pin.		
56	DH IN	I	V_{REF}	Intercom link input : • Intercom signals are input through a coupling capacitor C33 to this pin. • Input impedance is 10kΩ.		The input impedance as illustrated left and C33, C34, or C35 form a HPF.
57	RF1 IN	I	V_{REF}	RF1 link input : • RF1 signals are input through a coupling capacitor C34 to this pin. • Input impedance is 10kΩ.		
58	RF2 IN	I	V_{REF}	RF2 link input : • RF1 signals are input through a coupling capacitor C34 to this pin. • Input impedance is 10kΩ.		
59	PR	I	——	Power-ON reset control : • C36 between this pin and GND determines the power-ON reset time of the logic circuits.		• The larger C36, the longer the power-ON reset time. • The power-ON reset signal is output when the supply voltage reaches 4V.
60	V_{CC}	—	5V ±0.5V	External supply voltage input : • 5 ± 0.5 V power supply is input to this pin.	——	——
61	V_{reg}	O	V_{CC} – 0.2V DC 2V during power failure	Internal supply voltage output : • A power supply derived from line voltage is output from this pin to the internal speech network.		——
62	VLC	—	2-5 VDC depending on V_L	Circuit voltage control (2) : • This pin is grounded through C38.		C38 (typically 47µF) determines how the circuit voltage fluctuates.

■ Pin Descriptions (cont.)

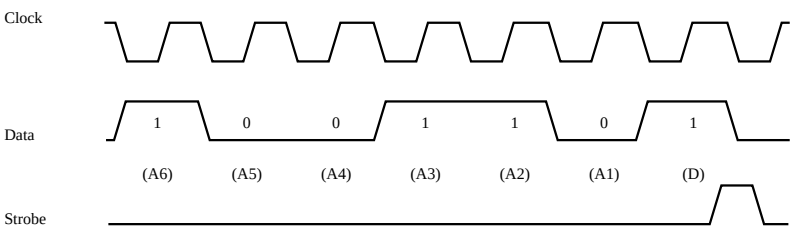
PinNo.	Symbol	I/O	Waveform	Description	Equivalent Circuit	Remarks
63	PD2	O	DC 0 to 3V depending on V_L	Line current bypass (2) : • Line current is bypassed from this pin through R39 to GND. R39 must be 1/2 W or more.		Z_{Tel} is 1.5 to 2kΩ on the IC side. It must be adjusted to 600Ω by inserting a 820Ω resistor between V_L and GND. 
64	PDI	I	DC Same as above $V_L - 33\Omega \times I_L$	Line current bypass (1) : • Line current is bypassed from this pin through R40 to Pinw. R40 must be 1/2 W or more.		

■ Logic Specifications

(Basic Block Diagrams)



Time charts (assuming the address h26 latch is to be set)



1. Data is read into the shift register in synchronization with a rising edge of the clock, with the higher data being shifted sequentially on a first-come highest-bit basis.
2. When the strobe is low, data is shifted sequentially on the sift register in synchronization with the clock. Data on the latch circuit will not change.
3. When the strobe goes high, the latched data whose address is represented by the highest 6-bit of the shift register is updated. Latched data is set when the least significant bit is 1, and reset when the bit is 0.
4. Referring to 3 above, if the address is h00 (the highest 6-bit of the shift register are all 0s), the latch circuit is cleared (all reset) regardless of the data content.
5. At power-on, the latch circuit is cleared (by power-ON reset).

■ Logic Circuits Address Specifications

1. Cross-point switch

Input \ Output	Handset rec.	Line output	Loudspeaker	Intercom	RF1	RF2	Recording	Time stamp
Loudspeaker	—	—	02	—	—	—	—	—
Microphone	—	09	0A	0B	0C	0D	0E	—
Receiver	10	—	12	—	14	15	16	—
Intercom	18	—	1A	—	1C	1D	1E	—
RF1	20	21	—	23	—	25	26	—
RF2	28	29	—	2B	2C	—	2E	—
MIX	30	31	32	33	34	35	—	37
AUX	38	39	3A	3B	3C	3D	3E	—

Note) Empty space means “not applicable.” Address is in hexadecimal.

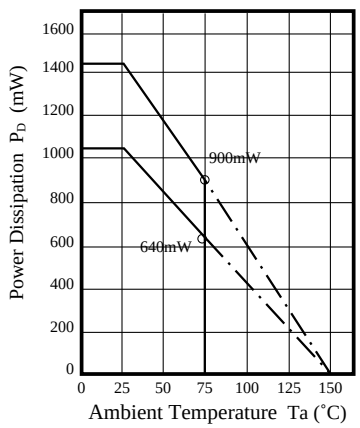
2. Other control switches

(Address)	(Description)
00	All reset
07	Recording amp. ON
0F	Playing amp. ON
17	Receiver volume 6 dB up
1F	Receiver volume 9 dB up (when address 17 is on)
27	Handset receiver amp. mute
2F	Loudspeaker amp. gain 12 dB down

Note) Address is in hexadecimal.

■ Package power dissipation

$P_D - Ta$



■ Application Circuit