Features

- **Full TCG/TCPA V1.1b Compatibility**
- **Single Chip Turnkey Solution**
- **Hardware Asymmetric Crypto Engine**
- **2048 RSA Sign in 500 ms Using CRT**
- **AVR 8-bit RISC Microprocessor**
- **Internal EEPROM Storage for 10+ RSA Keys**
- **33 MHz LPC (Low Pin Count) Bus for Easy PC Interface**
- **Secure Hardware and Firmware Design and Chip Layout**
- **True Random Number Generator (RNG)**
- **Secure Real-time Clock Option**
- **3.3V ±10% Supply Voltage**
- **28-lead TSSOP Package**
- **0–70°C Temperature Range**

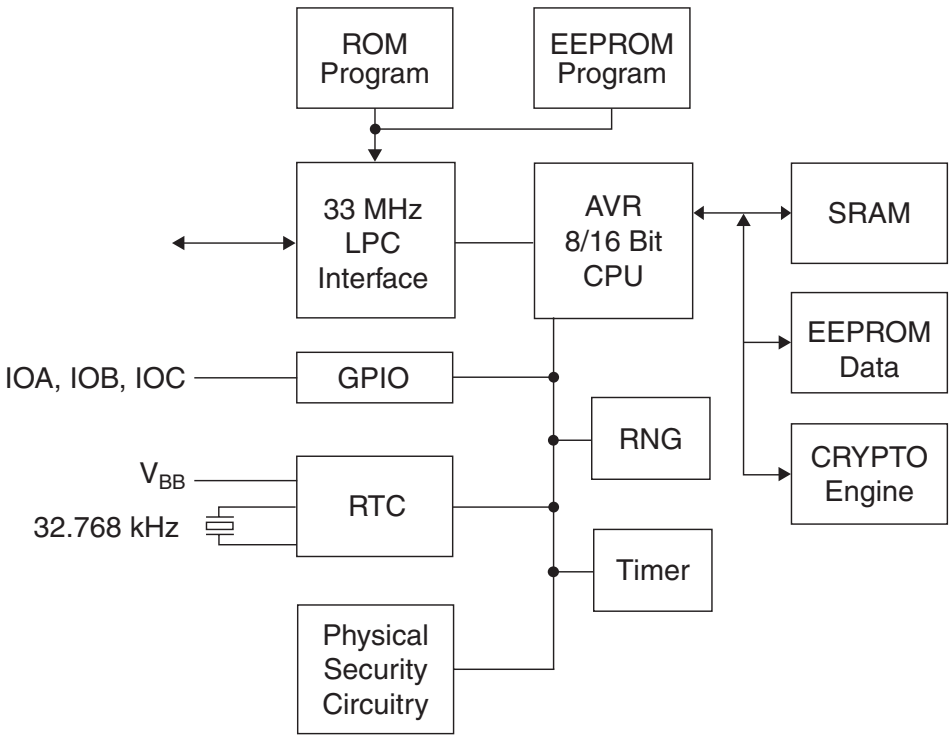
Description

The AT97SC3201 is a fully integrated security module designed to be integrated into personal computers and other embedded systems. It implements version 1.1b of the Trusted Computing Platform Alliance (TCPA) specification for Trusted Platform Modules (TPM). This specification has been adopted by the Trusted Computing Group (TCG).

The TPM includes a crypto accelerator capable of computing a 2048-bit RSA signature in 500 ms and a 1024-bit RSA signature in 100 ms, both using CRT.

The chip communicates with the PC through the LPC interface, which runs at 33 MHz. In addition, it supports SIRQ (for interrupts) and CLKRUN (to permit clock stopping).

Figure 1. AT97SC3201 Block Diagram



The chip includes a full hardware random number generator that is used for the TCG/TCPA protocol and is also available to the system for any random numbers it may need during normal operation.

Trusted Platform Module

AT97SC3201

Summary

Rev. 2015BS-TPM–04/03

A real-time clock function is available using an external battery and crystal. The chip provides tamper detection if the battery or crystal are removed or tampered with, and the current time value can be signed by the appropriate internal keys to verify its accuracy. (Contact Atmel for current status of this option.)

The battery detector can be used without the crystal for lower cost. In this mode, the TPM can indicate to the system if it has been removed from the PC in any way and can also take actions internally.

The chip uses a dynamic internal memory management scheme to store from 10 to 20 keys. Other than the standard TCG/TCPA commands (TPM_Evictkey, TPM_Loadkey), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary driver software for integration into certain operating systems, along with BIOS drivers. A TCG/TCPA Software Stack (TSS), also supplied by Atmel and available under license, provides communication support to any application using MSCAPI or PKCS #11 Cryptographic APIs. (Contact Atmel for a complete list of operating systems supported.)

Full documentation for TCG/TCPA primitives can be found on the TCG Web site, www.trustedcomputinggroup.org. This specification includes only mechanical, electrical and LPC protocol information.

Absolute Maximum Ratings

Operating Temperature.....0°C to +70°C
Storage Temperature (without Bias).....0°C to + 70°C
Voltage on I/O Pins.....–0.1 to V_{CC} +0.3V
Voltage on VCC with Respect to Ground.....6.0V
Maximum ESD Voltage.....2000V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification may cause temporary or permanent failure. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. DC Parameters

V_{CC} = 3.0 to 3.6V; Temperature = 0 to 70°C

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
I_{CC}	Operating Current at fclk = 33 MHz		25	50	mA	
I_{ST}	Static Current		5	10	mA	V_{CC} = 3.6V; fxtal = 0 Hz, active inputs
I_{SL}	Sleep Current, Chip Idle		40	100	µA	V_{CC} = 3.6V; fxtal = 0 Hz
I_{BB}	Battery Current		2	4	µA	V_{CC} = 0V; fxtal = 0 Hz.
I_{LIO}	Input Leakage		0.1	3	µA	Vin = V_{CC} or GND
V_{IH}	Input High Threshold	0.5 * V_{CC}		V_{CC} + 0.5	V	
V_{IL}	Input Low Threshold	–0.5		0.3 * V_{CC}	V	
V_{OH}	Output High Voltage	0.9 * V_{CC}	0.98 * V_{CC}		V	At I_{OUT} = –500 uA
V_{OL}	Output Low Voltage			0.1 * V_{CC}	V	At I_{OUT} = 1.5mA
I_{OLCR}	Output Low Current, CLKRUN#	7			mA	At V_{OUT} = .615 * V_{CC}
C_I	Input Pin Capacitance		6		pF	Note 1

Note: These parameters guaranteed but not tested.

Table 2. AC Parameters

Cl = 10pf. V_{CC} = 3.0 to 3.7V; Temperature = 0 to 70°C

Symbol	Parameter	Min	Nom	Max	Units	Notes
T_{VAL}	CLK to Signal Valid Delay – LAD0-3	2	5	11	ns	Measured at Vtrise = 0.285 * V_{CC} and Vtfal = 0.615 * V_{CC}. Measured from clk at Vtest = 0.4 * V_{CC}; Load = 200Ω
T_{ON}	Float to Active Delay	2	4		ns	
T_{OFF}	Active to Float Delay			28	ns	
T_{SU}	Input Setup Time to CLK	7	2		ns	
T_{H}	Input Hold Time from CLK	0	–500		ns	
T_{RST}	Reset Active Time after Power Stable	1			ms	Note 2
$T_{RST-CLK}$	Reset Active after CLK Stable	100			m	Note 2
$T_{RST-OFF}$	Reset Active to Output Float Delay			40	ns	Note 2
T_{CLKIN}	CLK Period	29.5	30	31	ns	Note 3
T_{CLKLO}	CLK Low Duration	13.4		18	ns	Note 1, Note 3
T_{CLKHI}	CLK High Duration	13.4		18	ns	Note 1, Note 3

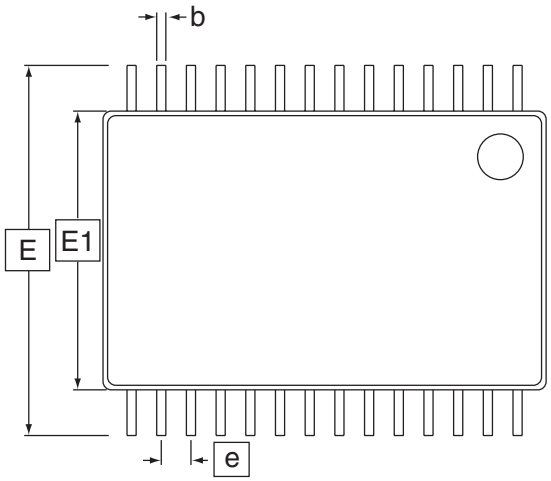
Note: 1. All parameters measured with respect to signal crossing Vtest = 0.4 * V_{CC} unless otherwise noted.
2. These parameters guaranteed but not tested.
3. The minimum parameter must never be violated under any circumstances unless Ireset# is asserted. If proper CLKRUN# signaling is observed, the maximum specification can be violated.

Table 3. Ordering Information

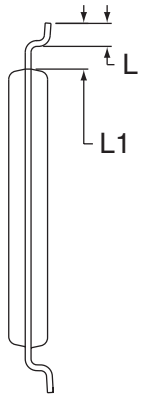
Ordering Code	Package	Operation Range
AT97SC3201-01AC	28A	Commercial (0° to 70° C)

Package Drawing

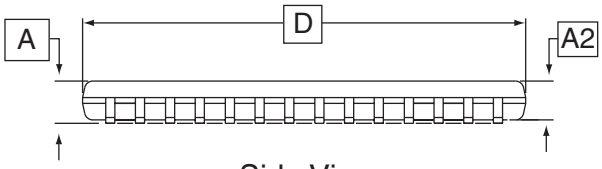
28A4 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	9.60	9.70	9.80	2, 5
E		8.10 BSC		
E1	6.00	6.10	6.20	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation DB for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

1/8/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28A3**, 28-lead, 6.1 x 9.7 mm Body, 0.65 pitch, Thin Shrink Small Outline Package (TSSOP)	28A3	A

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