

SBS 1.1-Compliant Gas Gauge and Protection Enabled With Impedance Track™

FEATURES

- **Next Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries**
 - **Better Than 1% Error Over the Lifetime of the Battery**
- **Supports the Smart Battery Specification SBS V1.1**
- **Flexible Configuration for 2 to 4 Series Li-Ion and Li-Polymer Cells**
- **Powerful 8-Bit RISC CPU With Ultralow Power Modes**
- **Full Array of Programmable Protection Features**
 - **Voltage, Current, and Temperature**
- **Satisfies JEITA Guidelines**
- **Added Flexibility to Handle More Complex Charging Profiles**
- **Lifetime Data Logging**
- **Supports SHA-1 Authentication**
- **Complete Battery Protection and Gas Gauge Solution in One Package**
- **Available in a 38-Pin TSSOP (DBT) package**

DESCRIPTION

The bq20z45 SBS-compliant gas gauge and protection IC is a single IC solution designed for battery-pack or in-system installation. The bq20z45 measures and maintains an accurate record of available charge in Li-ion or Li-polymer batteries using its integrated high-performance analog peripherals, monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack as well and reports the information to the system host controller over a serial-communication bus. Together with the integrated analog front-end (AFE) short-circuit and overload protection, the bq20z45 maximizes functionality and safety while minimizing external component count, cost, and size in smart battery circuits.

The implemented Impedance Track™ gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging all accounted for during each stage of every cycle with high accuracy.

APPLICATIONS

- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

AVAILABLE OPTIONS

T _A	PACKAGE ⁽¹⁾	
	38-PIN TSSOP (DBT) Tube	38-PIN TSSOP (DBT) Tape and Reel
–40°C to 85°C	bq20z45DBT ⁽²⁾	bq20z45DBTR ⁽³⁾

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) A single tube quantity is 50 units.

(3) A single reel quantity is 2000 units



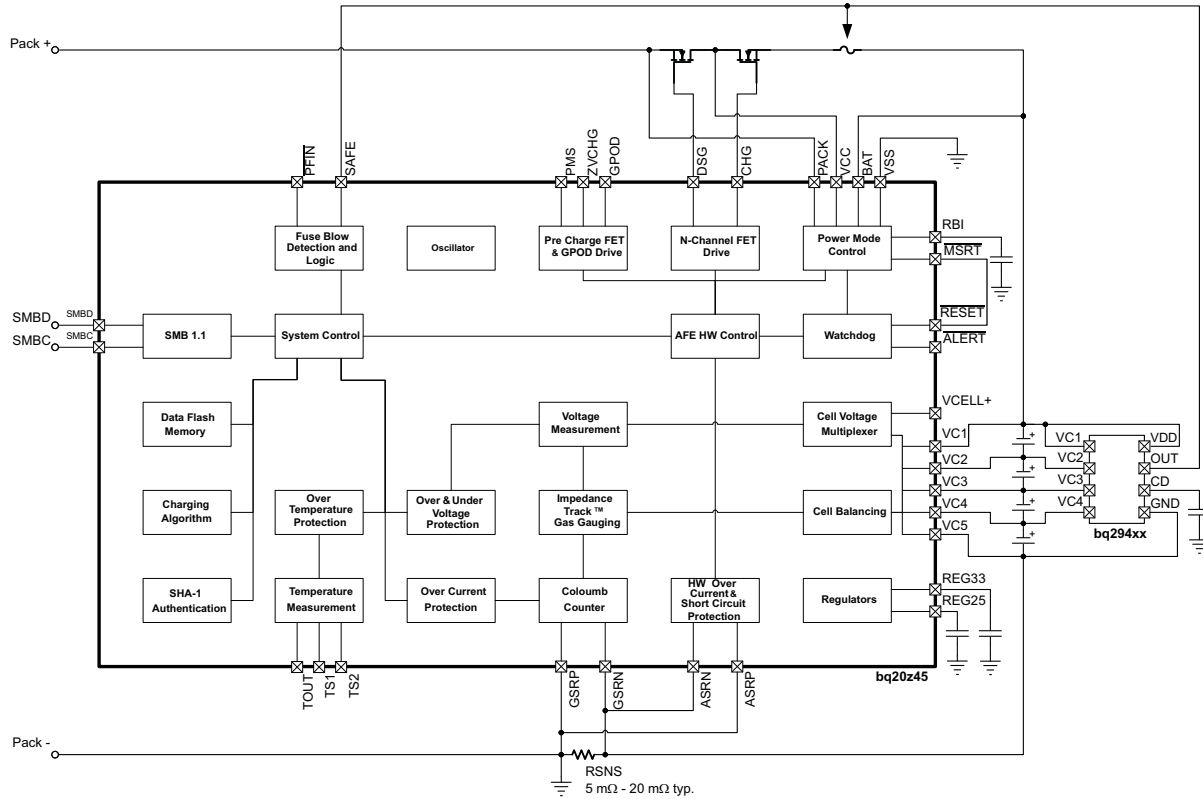
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Impedance Track is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM PARTITIONING DIAGRAM



**bq20z45
DBT PACKAGE
(TOP VIEW)**

DSG	1	38	CHG
PACK	2	37	BAT
VCC	3	36	VC1
ZVCHG	4	35	VC2
GPOD	5	34	VC3
PMS	6	33	VC4
VSS	7	32	VC5
REG33	8	31	ASRP
TOUT	9	30	ASRN
VCELL+	10	29	RESET
ALERT	11	28	VSS
PRES	12	27	RBI
TS1	13	26	REG25
TS2	14	25	VSS
PFIN	15	24	MRST
SAFE	16	23	GSRN
SMBD	17	22	GSRP
SMBC	18	21	VSS
NC	19	20	VSS

PIN FUNCTIONS

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	DSG	O	High side N-chan discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in shutdown mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input
4	ZVCHG	O	P-chan pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. Can be configured to be used in pre-charge condition
6	PMS	I	Pre-charge mode setting input. Connect to PACK to enable 0v pre-charge using charge FET connected at CHG pin. Connect to VSS to disable 0V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device
8	REG33	P	3.3V regulator output. Connect at least a 2.2μF capacitor to REG33 and VSS
9	TOUT	P	Thermistor bias supply output
10	VCELL+	-	Internal cell voltage multiplexer and amplifier output. Connect a 0.1μF capacitor to VCELL+ and VSS
11	$\overline{\text{ALERT}}$	I/OD	Alert output. In case of short circuit condition, overload condition and watchdog time out this pin will be triggered.
12	$\overline{\text{PRES}}$	I/OD	System / Host present input. Pull up to TOUT
13	TS1	IA	Temperature sensor 1 input
14	TS2	IA	Temperature sensor 2 input
15	$\overline{\text{PFIN}}$	I/OD	Fuse blow detection input
16	SAFE	I/OD	blow fuse signal output
17	SMBD	I/OD	SMBus data line
18	SMBC	I/OD	SMBus clock line
19	NC	-	Not connected
20, 21, 25, 28	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device
22	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor
23	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor
24	$\overline{\text{MRST}}$	I	Reset input for internal CPU core. connect to $\overline{\text{RESET}}$ for correct operation of device
26	REG25	P	2.5V regulator output. Connect at least a 1μF capacitor to REG25 and VSS
27	RBI	P	RAM backup input. Connect a capacitor to this pin and VSS to protect loss of RAM data in case of short circuit condition
29	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MRST}}$.
30	ASRN	IA	Short circuit and overload detection differential input. Connect to sense resistor
31	ASRP	IA	Short circuit and overload detection differential input. Connect to sense resistor
32	VC5	IA, P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in cell stack.
33	VC4	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in cell stack.
34	VC3	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in cell stack and the negative voltage of the second highest cell in 4 cell applications.
35	VC2	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4 cell applications. Connect to VC3 in 2 cell stack applications
36	VC1	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the highest cell in cell stack in 4 cell applications. Connect to VC2 in 3 or 2 cell stack applications
37	BAT	I, P	Battery stack voltage sense input
38	CHG	O	High side N-chan charge FET gate drive

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

	PIN	UNIT
V _{SS} Supply voltage range	BAT, VCC	–0.3 V to 34 V
	PACK, PMS	–0.3 V to 34 V
	VC(n)-VC(n+1); n = 1, 2, 3, 4	–0.3 V to 8.5 V
	VC1, VC2, VC3, VC4	–0.3 V to 34 V
	VC5	–0.3 V to 1 V
V _{IN} Input voltage range	$\overline{\text{PFIN}}$, SMBD, SMBC	–0.3 V to 6 V
	TS1, TS2, SAFE, VCELL+, $\overline{\text{PRES}}$, $\overline{\text{ALERT}}$	–0.3 V to V _(REG25) + 0.3 V
	$\overline{\text{MRST}}$, GSRN, GSRP, RBI	–0.3 V to V _(REG25) + 0.3 V
	ASRN, ASRP	–1 V to 1 V
V _{OUT} Output voltage range	DSG, CHG, GPOD	–0.3 V to 34 V
	ZVCHG	–0.3 V to V _(BAT)
	TOUT, $\overline{\text{ALERT}}$, REG33	–0.3 V to 6 V
	$\overline{\text{RESET}}$	–0.3 V to 7 V
	REG25	–0.3 V to 2.75 V
I _{SS} Maximum combined sink current for input pins	$\overline{\text{PRES}}$, $\overline{\text{PFIN}}$, SMBD, SMBC	50 mA
T _A Operating free-air temperature range		–40°C to 85°C
T _F Functional temperature		–40°C to 100°C
T _{stg} Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	PIN	MIN	NOM	MAX	UNIT
V _{SS} Supply voltage	VCC, BAT	4.5		25	V
V _(STARTUP) Minimum startup voltage	VCC, BAT, PACK	5.5			V
V _{IN} Input Voltage Range	VC(n)-VC(n+1); n = 1,2,3,4	0		5	V
	VC1, VC2, VC3, VC4	0		V _{SUP}	V
	VC5	0		0.5	V
	ASRN, ASRP	–0.5		0.5	V
	PACK, PMS	0		25	V
V _(GPOD) Output Voltage Range	GPOD	0		25	V
A _(GPOD) Drain Current ⁽¹⁾	GPOD			1	mA
C _(REG25) 2.5V LDO Capacitor	REG25	1			μF
C _(REG33) 3.3V LDO Capacitor	REG33	2.2			μF
C _(VCELL+) Cell Voltage Output Capacitor	VCELL+	0.1			μF
C _(PACK) PACK input block resistor ⁽²⁾	PACK	1			kΩ

(1) Use an external resistor to limit the current to GPOD to 1mA in high voltage application.

(2) Use an external resistor to limit the inrush current PACK pin required.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted), $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{(\text{REG25})} = 2.41\text{ V}$ to 2.59 V , $V_{(\text{BAT})} = 14\text{ V}$, $C_{(\text{REG25})} = 1\text{ }\mu\text{F}$, $C_{(\text{REG33})} = 2.2\text{ }\mu\text{F}$; typical values at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(\text{NORMAL})}$	Firmware running			550		μA
$I_{(\text{SLEEP})}$	Sleep Mode	CHG FET on; DSG FET on		124		μA
		CHG FET off; DSG FET on		90		μA
		CHG FET off; DSG FET off		52		μA
$I_{(\text{SHUTDOWN})}$	Shutdown Mode		0.1		1	μA
SHUTDOWN WAKE; $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$I_{(\text{PACK})}$	Shutdown exit at V_{STARTUP} threshold				1	μA
SRx WAKE FROM SLEEP; $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$V_{(\text{WAKE})}$	Positive or negative wake threshold with 1.00 mV, 2.25 mV, 4.5 mV and 9 mV programmable options		1.25		10	mV
$V_{(\text{WAKE_ACR})}$	Accuracy of $V_{(\text{WAKE})}$	$V_{(\text{WAKE})} = 1\text{ mV};$ $I_{(\text{WAKE})} = 0, \text{RSNS1} = 0, \text{RSNS0} = 1;$	-0.7		0.7	mV
		$V_{(\text{WAKE})} = 2.25\text{ mV};$ $I_{(\text{WAKE})} = 1, \text{RSNS1} = 0, \text{RSNS0} = 1;$ $I_{(\text{WAKE})} = 0, \text{RSNS1} = 1, \text{RSNS0} = 0;$	-0.8		0.8	
		$V_{(\text{WAKE})} = 4.5\text{ mV};$ $I_{(\text{WAKE})} = 1, \text{RSNS1} = 1, \text{RSNS0} = 1;$ $I_{(\text{WAKE})} = 0, \text{RSNS1} = 1, \text{RSNS0} = 0;$	-1.0		1.0	
		$V_{(\text{WAKE})} = 9\text{ mV};$ $I_{(\text{WAKE})} = 1, \text{RSNS1} = 1, \text{RSNS0} = 1;$	-1.4		1.4	
$V_{(\text{WAKE_TCO})}$	Temperature drift of $V_{(\text{WAKE})}$ accuracy			0.5		$\%/^{\circ}\text{C}$
$t_{(\text{WAKE})}$	Time from application of current and wake of bq8040			1	10	ms
POWER-ON RESET						
$V_{\text{IT-}}$	Negative-going voltage input	Voltage at REG25 pin	1.70	1.80	1.90	V
V_{hys}	Hysteresis	$V_{\text{IT+}} - V_{\text{IT-}}$	50	150	250	mV
t_{RST}	$\overline{\text{RESET}}$ active low time	active low time after power up or watchdog reset	100	250	560	μs
WATCHDOG TIMER						
t_{WDTINT}	Watchdog start up detect time		250	500	1000	ms
t_{WDWT}	Watchdog detect time		50	100	150	μs
2.5V LDO; $I_{(\text{REG33OUT})} = 0\text{ mA}; T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$V_{(\text{REG25})}$	Regulator output voltage	$4.5 < \text{VCC or BAT} < 25\text{ V};$ $I_{(\text{REG25OUT})} \leq 16\text{ mA};$ $T_A = -40^{\circ}\text{C to } 100^{\circ}\text{C}$	2.41	2.5	2.59	V
$\Delta V_{(\text{REG25TEMP})}$	Regulator output change with temperature	$I_{(\text{REG25OUT})} = 2\text{ mA};$ $T_A = -40^{\circ}\text{C to } 100^{\circ}\text{C}$		± 0.2		%
$\Delta V_{(\text{REG25LINE})}$	Line regulation	$5.4 < \text{VCC or BAT} < 25\text{ V};$ $I_{(\text{REG25OUT})} = 2\text{ mA}$		3	10	mV
$\Delta V_{(\text{REG25LOAD})}$	Load Regulation	$0.2\text{ mA} \leq I_{(\text{REG25OUT})} \leq 2\text{ mA}$		7	25	mV
		$0.2\text{ mA} \leq I_{(\text{REG25OUT})} \leq 16\text{ mA}$		25	50	
$I_{(\text{REG25MAX})}$	Current Limit	drawing current until REG25 = 2 V to 0 V	5	40	75	mA
3.3V LDO; $I_{(\text{REG25OUT})} = 0\text{ mA}; T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$V_{(\text{REG33})}$	Regulator output voltage	$4.5 < \text{VCC or BAT} < 25\text{ V};$ $I_{(\text{REG33OUT})} \leq 25\text{ mA};$ $T_A = -40^{\circ}\text{C to } 100^{\circ}\text{C}$	3	3.3	3.6	V
$\Delta V_{(\text{REG33TEMP})}$	Regulator output change with temperature	$I_{(\text{REG33OUT})} = 2\text{ mA};$ $T_A = -40^{\circ}\text{C to } 100^{\circ}\text{C}$		± 0.2		%
$\Delta V_{(\text{REG33LINE})}$	Line regulation	$5.4 < \text{VCC or BAT} < 25\text{ V};$ $I_{(\text{REG33OUT})} = 2\text{ mA}$		3	10	mV
$\Delta V_{(\text{REG33LOAD})}$	Load Regulation	$0.2\text{ mA} \leq I_{(\text{REG33OUT})} \leq 2\text{ mA}$		7	17	mV
		$0.2\text{ mA} \leq I_{(\text{REG33OUT})} \leq 25\text{ mA}$		40	100	

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted), $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{(\text{REG25})} = 2.41\text{ V}$ to 2.59 V , $V_{(\text{BAT})} = 14\text{ V}$, $C_{(\text{REG25})} = 1\text{ }\mu\text{F}$, $C_{(\text{REG33})} = 2.2\text{ }\mu\text{F}$; typical values at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(\text{REG33MAX})}$	Current Limit	drawing current until REG33 = 3 V	25	100	145	mA
		short REG33 to VSS, REG33 = 0 V	12		65	
THERMISTOR DRIVE						
$V_{(\text{TOUT})}$	Output voltage	$I_{(\text{TOUT})} = 0\text{ mA}$; $T_A = 25^{\circ}\text{C}$		$V_{(\text{REG25})}$		V
$R_{\text{DS(on)}}$	TOUT pass element resistance	$I_{(\text{TOUT})} = 1\text{ mA}$; $R_{\text{DS(on)}} = (V_{(\text{REG25})} - V_{(\text{TOUT})}) / 1\text{ mA}$; $T_A = -40^{\circ}\text{C}$ to 100°C		50	100	Ω
VCELL+ HIGH VOLTAGE TRANSLATION						
$V_{(\text{VCELL+OUT})}$	Translation output	$VC(n) - VC(n+1) = 0\text{ V}$; $T_A = -40^{\circ}\text{C}$ to 100°C	0.950	0.975	1	V
		$VC(n) - VC(n+1) = 4.5\text{ V}$; $T_A = -40^{\circ}\text{C}$ to 100°C	0.275	0.3	0.375	
$V_{(\text{VCELL+REF})}$	Translation output	internal AFE reference voltage ; $T_A = -40^{\circ}\text{C}$ to 100°C	0.965	0.975	0.985	
$V_{(\text{VCELL+PACK})}$		Voltage at PACK pin; $T_A = -40^{\circ}\text{C}$ to 100°C	$0.98 \times V_{(\text{PACK})}/18$	$V_{(\text{PACK})}/18$	$1.02 \times V_{(\text{PACK})}/18$	
$V_{(\text{VCELL+BAT})}$	Voltage at BAT pin; $T_A = -40^{\circ}\text{C}$ to 100°C	$0.98 \times V_{(\text{BAT})}/18$	$V_{(\text{BAT})}/18$	$1.02 \times V_{(\text{BAT})}/18$		
CMMR	Common mode rejection ratio	VCELL+	40			dB
K	Cell scale factor	$K = \{V_{\text{CELL+ output}}(VC5=0V$; $VC4=4.5V) - V_{\text{CELL+ output}}(VC5=0V$; $VC4=0V)\}/4.5$	0.147	0.150	0.153	
		$K = \{V_{\text{CELL+ output}}(VC2=13.5V$; $VC1=18V) - V_{\text{CELL+ output}}(VC5=13.5V$; $VC1=13.5V)\}/4.5$	0.147	0.150	0.153	
$I_{(\text{VCELL+OUT})}$	Drive Current to VCELL+ capacitor	$VC(n) - VC(n+1) = 0V$; $V_{\text{CELL+}} = 0\text{ V}$; $T_A = -40^{\circ}\text{C}$ to 100°C	12	18		μA
$V_{(\text{VCELL+O})}$	CELL offset error	CELL output ($VC2 = VC1 = 18\text{ V}$) - CELL output ($VC2 = VC1 = 0\text{ V}$)	-18	-1	18	mV
I_{VcnL}	VC(n) pin leakage current	VC1, VC2, VC3, VC4, VC5 = 3 V	-1	0.01	1	μA
CELL BALANCING						
$R_{(\text{BAL})}$	internal cell balancing FET resistance	$R_{\text{DS(on)}}$ for internal FET switch at $V_{\text{DS}} = 2\text{ V}$; $T_A = 25^{\circ}\text{C}$	200	400	600	Ω
HARDWARE SHORT CIRCUIT AND OVERLOAD PROTECTION; $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$V_{(\text{OL})}$	OL detection threshold voltage accuracy	$V_{\text{OL}} = 25\text{ mV (min)}$	15	25	35	mV
		$V_{\text{OL}} = 100\text{ mV}$; $RSNS = 0, 1$	90	100	110	
		$V_{\text{OL}} = 205\text{ mV (max)}$	185	205	225	
$V_{(\text{SCC})}$	SCC detection threshold voltage accuracy	$V_{(\text{SCC})} = 50\text{ mV (min)}$	30	50	70	mV
		$V_{(\text{SCC})} = 200\text{ mV}$; $RSNS = 0, 1$	180	200	220	
		$V_{(\text{SCC})} = 475\text{ mV (max)}$	428	475	523	
$V_{(\text{SCD})}$	SCD detection threshold voltage accuracy	$V_{(\text{SCD})} = -50\text{ mV (min)}$	-30	-50	-70	mV
		$V_{(\text{SCD})} = -200\text{ mV}$; $RSNS = 0, 1$	-180	-200	-220	
		$V_{(\text{SCD})} = -475\text{ mV (max)}$	-428	-475	-523	
t_{da}	Delay time accuracy		± 15.25			μs
t_{pd}	Protection circuit propagation delay		50			μs
FET DRIVE CIRCUIT; $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)						
$V_{(\text{DSGON})}$	DSG pin output on voltage	$V_{(\text{DSGON})} = V_{(\text{DSG})} - V_{(\text{PACK})}$; $V_{(\text{GS})} = 10\text{ M}\Omega$; DSG and CHG on; $T_A = -40^{\circ}\text{C}$ to 100°C	8	12	16	V
$V_{(\text{CHGON})}$	CHG pin output on voltage	$V_{(\text{CHGON})} = V_{(\text{CHG})} - V_{(\text{BAT})}$; $V_{(\text{GS})} = 10\text{ M}\Omega$; DSG and CHG on; $T_A = -40^{\circ}\text{C}$ to 100°C	8	12	16	V
$V_{(\text{DSGOFF})}$	DSG pin output off voltage	$V_{(\text{DSGOFF})} = V_{(\text{DSG})} - V_{(\text{PACK})}$			0.2	V
$V_{(\text{CHGOFF})}$	CHG pin output off voltage	$V_{(\text{CHGOFF})} = V_{(\text{CHG})} - V_{(\text{BAT})}$			0.2	V

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted), $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{(\text{REG25})} = 2.41\text{ V}$ to 2.59 V , $V_{(\text{BAT})} = 14\text{ V}$, $C_{(\text{REG25})} = 1\text{ }\mu\text{F}$, $C_{(\text{REG33})} = 2.2\text{ }\mu\text{F}$; typical values at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$C_L = 4700\text{ pF}$; $V_{(\text{PACK})} \leq \text{DSG} \leq V_{(\text{PACK})} + 4\text{ V}$		400	1000	μs
		$C_L = 4700\text{ pF}$; $V_{(\text{BAT})} \leq \text{CHG} \leq V_{(\text{BAT})} + 4\text{ V}$		400	1000	
t_f	Fall time	$C_L = 4700\text{ pF}$; $V_{(\text{PACK})} + V_{(\text{DSGON})} \leq \text{DSG} \leq V_{(\text{PACK})} + 1\text{ V}$		40	200	μs
		$C_L = 4700\text{ pF}$; $V_{(\text{BAT})} + V_{(\text{CHGON})} \leq \text{CHG} \leq V_{(\text{BAT})} + 1\text{ V}$		40	200	
$V_{(\text{ZVCHG})}$	ZVCHG clamp voltage	BAT = 4.5 V	3.3	3.5	3.7	V
LOGIC; $T_A = -40^{\circ}\text{C}$ to 100°C (unless otherwise noted)						
$R_{(\text{PULLUP})}$	Internal pullup resistance	$\overline{\text{ALERT}}$	60	100	200	k Ω
		$\overline{\text{RESET}}$	1	3	6	
V_{OL}	Logic low output voltage level	$\overline{\text{ALERT}}$			0.2	V
		$\overline{\text{RESET}}$; $V_{(\text{BAT})} = 7\text{ V}$; $V_{(\text{REG25})} = 1.5\text{ V}$; $I_{(\text{RESET})} = 200\text{ }\mu\text{A}$			0.4	
		GPOD; $I_{(\text{GPOD})} = 50\text{ }\mu\text{A}$			0.6	
LOGIC SMBC, SMBD, PFIN, PRES, SAFE, ALERT						
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	Output voltage high ⁽¹⁾	$I_L = -0.5\text{ mA}$	$V_{\text{REG25}} - 0.5$			V
V_{OL}	Low-level output voltage	$\overline{\text{PRES}}$, $\overline{\text{PFIN}}$, $\overline{\text{ALERT}}$, $I_L = 7\text{ mA}$;			0.4	V
C_i	Input capacitance			5		pF
$I_{(\text{SAFE})}$	SAFE source currents	SAFE active, $\text{SAFE} = V_{(\text{REG25})} - 0.6\text{ V}$	-3			mA
I_{ikg}	SAFE leakage current	SAFE inactive	-0.2		0.2	μA
	Input leakage current				1	μA
ADC⁽²⁾						
	Input voltage range	TS1, TS2, using Internal V_{ref}	-0.2		1	V
	Conversion time			31.5		ms
	Resolution (no missing codes)		16			bits
	Effective resolution		14	15		bits
	Integral nonlinearity				± 0.03	%FSR ⁽³⁾
	Offset error ⁽⁴⁾			140	250	μV
	Offset error drift ⁽⁴⁾	$T_A = 25^{\circ}\text{C}$ to 85°C		2.5	18	$\mu\text{V}/^{\circ}\text{C}$
	Full-scale error ⁽⁵⁾			$\pm 0.1\%$	$\pm 0.7\%$	
	Full-scale error drift			50		PPM/ $^{\circ}\text{C}$
	Effective input resistance ⁽⁶⁾		8			M Ω
COULOMB COUNTER						
	Input voltage range		-0.20		0.20	V
	Conversion time	Single conversion		250		ms
	Effective resolution	Single conversion	15			bits
	Integral nonlinearity	-0.1 V to 0.20 V		± 0.007	± 0.034	%FSR
		-0.20 V to -0.1 V		± 0.007		

(1) RC[0:7] bus

(2) Unless otherwise specified, the specification limits are valid at all measurement speed modes

(3) Full-scale reference

(4) Post-calibration performance and no I/O changes during conversion with SRN as the ground reference

(5) Uncalibrated performance. This gain error can be eliminated with external calibration.

(6) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted), $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{(\text{REG}25)} = 2.41\text{ V}$ to 2.59 V , $V_{(\text{BAT})} = 14\text{ V}$, $C_{(\text{REG}25)} = 1\text{ }\mu\text{F}$, $C_{(\text{REG}33)} = 2.2\text{ }\mu\text{F}$; typical values at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset error ⁽⁷⁾	$T_A = 25^{\circ}\text{C}$ to 85°C		10		μV
Offset error drift			0.4	0.7	$\mu\text{V}/^{\circ}\text{C}$
Full-scale error ⁽⁸⁾⁽⁹⁾			$\pm 0.35\%$		
Full-scale error drift			150		PPM/ $^{\circ}\text{C}$
Effective input resistance ⁽¹⁰⁾	$T_A = 25^{\circ}\text{C}$ to 85°C	2.5			M Ω
INTERNAL TEMPERATURE SENSOR					
$V_{(\text{TEMP})}$ Temperature sensor voltage ⁽¹¹⁾			-2.0		mV/ $^{\circ}\text{C}$
VOLTAGE REFERENCE					
Output voltage		1.215	1.225	1.230	V
Output voltage drift			65		PPM/ $^{\circ}\text{C}$
HIGH FREQUENCY OSCILLATOR					
$f_{(\text{OSC})}$ Operating frequency			4.194		MHz
$f_{(\text{EIO})}$ Frequency error ⁽¹²⁾⁽¹³⁾		-3%	0.25%	3%	
	$T_A = 20^{\circ}\text{C}$ to 70°C	-2%	0.25%	2%	
$t_{(\text{SXO})}$ Start-up time ⁽¹⁴⁾			2.5	5	ms
LOW FREQUENCY OSCILLATOR					
$f_{(\text{LOSC})}$ Operating frequency			32.768		kHz
$f_{(\text{LEIO})}$ Frequency error ⁽¹³⁾⁽¹⁵⁾		-2.5%	0.25%	2.5%	
	$T_A = 20^{\circ}\text{C}$ to 70°C	-1.5%	0.25%	1.5%	
$t_{(\text{LSXO})}$ Start-up time ⁽¹⁴⁾				500	μs

(7) Post-calibration performance

(8) Reference voltage for the coulomb counter is typically $V_{\text{ref}}/3.969$ at $V_{(\text{REG}25)} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

(9) Uncalibrated performance. This gain error can be eliminated with external calibration.

(10) The CC input is a switched capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

(11) $-53.7\text{ LSB}/^{\circ}\text{C}$

(12) The frequency error is measured from 4.194 MHz.

(13) The frequency drift is included and measured from the trimmed frequency at $V_{(\text{REG}25)} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$

(14) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$

(15) The frequency error is measured from 32.768 kHz.

DATA FLASH CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Typical Values at $T_A = 25^\circ\text{C}$ and $V_{(\text{REG25})} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention	See ⁽¹⁾	10			Years
Flash programming write-cycles		20k			Cycles
$t_{(\text{ROWPROG})}$ Row programming time				2	ms
$t_{(\text{MASSERASE})}$ Mass-erase time				200	ms
$t_{(\text{PAGEERASE})}$ Page-erase time				20	ms
$I_{(\text{DDPROG})}$ Flash-write supply current				5	10
$I_{(\text{DDERASE})}$ Flash-erase supply current			5	10	mA
RAM BACKUP					
$I_{(\text{RB})}$ RB data-retention input current	$V_{(\text{RBI})} > V_{(\text{RBI})\text{MIN}}$, $V_{\text{REG25}} < V_{\text{IT-}}$, $T_A = 85^\circ\text{C}$		1000	2500	nA
	$V_{(\text{RBI})} > V_{(\text{RBI})\text{MIN}}$, $V_{\text{REG25}} < V_{\text{IT-}}$, $T_A = 25^\circ\text{C}$		90	220	
$V_{(\text{RB})}$ RB data-retention input voltage ⁽¹⁾		1.7			V

(1) Specified by design. Not production tested.

SMBus TIMING CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to 85°C Typical Values at $T_A = 25^\circ\text{C}$ and $V_{\text{REG25}} = 2.5\text{ V}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(\text{SMB})}$ SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
$f_{(\text{MAS})}$ SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(\text{BUF})}$ Bus free time between start and stop (see Figure 1)		4.7			μs
$t_{(\text{HD:STA})}$ Hold time after (repeated) start (see Figure 1)		4			μs
$t_{(\text{SU:STA})}$ Repeated start setup time (see Figure 1)		4.7			μs
$t_{(\text{SU:STO})}$ Stop setup time (see Figure 1)		4			μs
$t_{(\text{HD:DAT})}$ Data hold time (see Figure 1)	Receive mode	0			ns
	Transmit mode	300			
$t_{(\text{SU:DAT})}$ Data setup time (see Figure 1)		250			ns
$t_{(\text{TIMEOUT})}$ Error signal/detect (see Figure 1)	See ⁽¹⁾	25		35	μs
$t_{(\text{LOW})}$ Clock low period (see Figure 1)		4.7			μs
$t_{(\text{HIGH})}$ Clock high period (see Figure 1)	See ⁽²⁾	4		50	μs
$t_{(\text{LOW:SEXT})}$ Cumulative clock low slave extend time	See ⁽³⁾			25	ms
$t_{(\text{LOW:MEXT})}$ Cumulative clock low master extend time (see Figure 1)	See ⁽⁴⁾			10	ms
t_f Clock/data fall time	See ⁽⁵⁾			300	ns
t_r Clock/data rise time	See ⁽⁶⁾			1000	ns

(1) The bq8040 times out when any clock low exceeds $t_{(\text{TIMEOUT})}$.

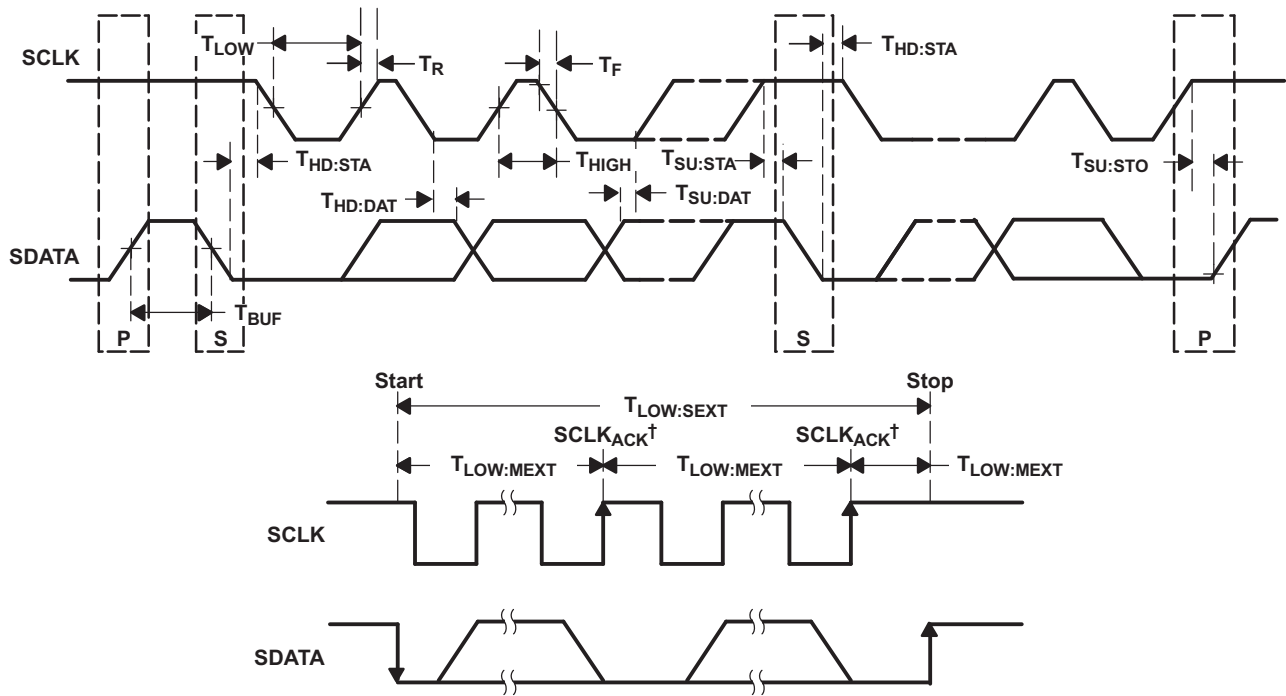
(2) $t_{(\text{HIGH})}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for $t > 50\text{ ms}$ causes reset of any transaction involving bq8040 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).

(3) $t_{(\text{LOW:SEXT})}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

(4) $t_{(\text{LOW:MEXT})}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

(5) Rise time $t_r = V_{\text{ILMAX}} - 0.15$ to $(V_{\text{IHMIN}} + 0.15)$

(6) Fall time $t_f = 0.9V_{\text{DD}}$ to $(V_{\text{ILMAX}} - 0.15)$



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

FEATURE SET

Primary (1st Level) Safety Features

The bq20z45 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short Circuit
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq20z45 can be used to indicate more serious faults via the SAFE (pin 7). This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and 0 Volt Charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- AFE communication fault

Charge Control Features

The bq20z45 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into 2 sub-ranges and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Determines the chemical state of charge of each battery cell using Impedance Track™ and can reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms.

Gas Gauging

The bq20z45 uses the Impedance Track™ Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note ([SLUA364](#)) for further details.

Lifetime Data Logging Features

The bq20z45 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored include:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power
- Lifetime average temperature

Authentication

The bq20z45 supports authentication by the host using SHA-1.

Power Modes

The bq20z45 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the bq20z45 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq20z45 is in a reduced power stage.
- In Sleep Mode, the bq20z45 performs measurements, calculations, protection decisions and data update in adjustable time intervals. Between these intervals, the bq20z45 is in a reduced power stage. The bq20z45 has a wake function that enables exit from Sleep mode, when current flow or failure is detected.
- In Shutdown Mode the bq20z45 is completely disabled.

CONFIGURATION

Oscillator Function

The bq20z45 fully integrates the system oscillators. Therefore the bq20z45 requires no external components for this feature.

System Present Operation

The bq20z45 checks the $\overline{\text{PRES}}$ pin periodically (1s). If $\overline{\text{PRES}}$ input is pulled to ground by external system, the bq20z45 detects this as system present.

BATTERY PARAMETER MEASUREMENTS

The bq20z45 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from -0.25 V to 0.25 V. The bq20z45 detects charge activity when $V_{\text{SR}} = V_{(\text{SRP})} - V_{(\text{SRN})}$ is positive and discharge activity when $V_{\text{SR}} = V_{(\text{SRP})} - V_{(\text{SRN})}$ is negative. The bq20z45 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq20z45 updates the individual series cell voltages at one second intervals. The internal ADC of the bq20z45 measures the voltage, scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track™ gas-gauging.

Current

The bq20z45 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5 mΩ to 20 mΩ typ. sense resistor.

Auto Calibration

The bq20z45 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq20z45 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq20z45 has an internal temperature sensor and inputs for 2 external temperature sensor inputs TS1 and TS2 used in conjunction with two identical NTC thermistors (default are Semitec 103AT) to sense the battery environmental temperature. The bq20z45 can be configured to use internal or up to 2 external temperature sensors.

COMMUNICATIONS

The bq20z45 uses SMBus v1.1 with Master Mode and package error checking (PEC) options per the SBS specification.

SMBus On and Off State

The bq20z45 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

SBS Commands

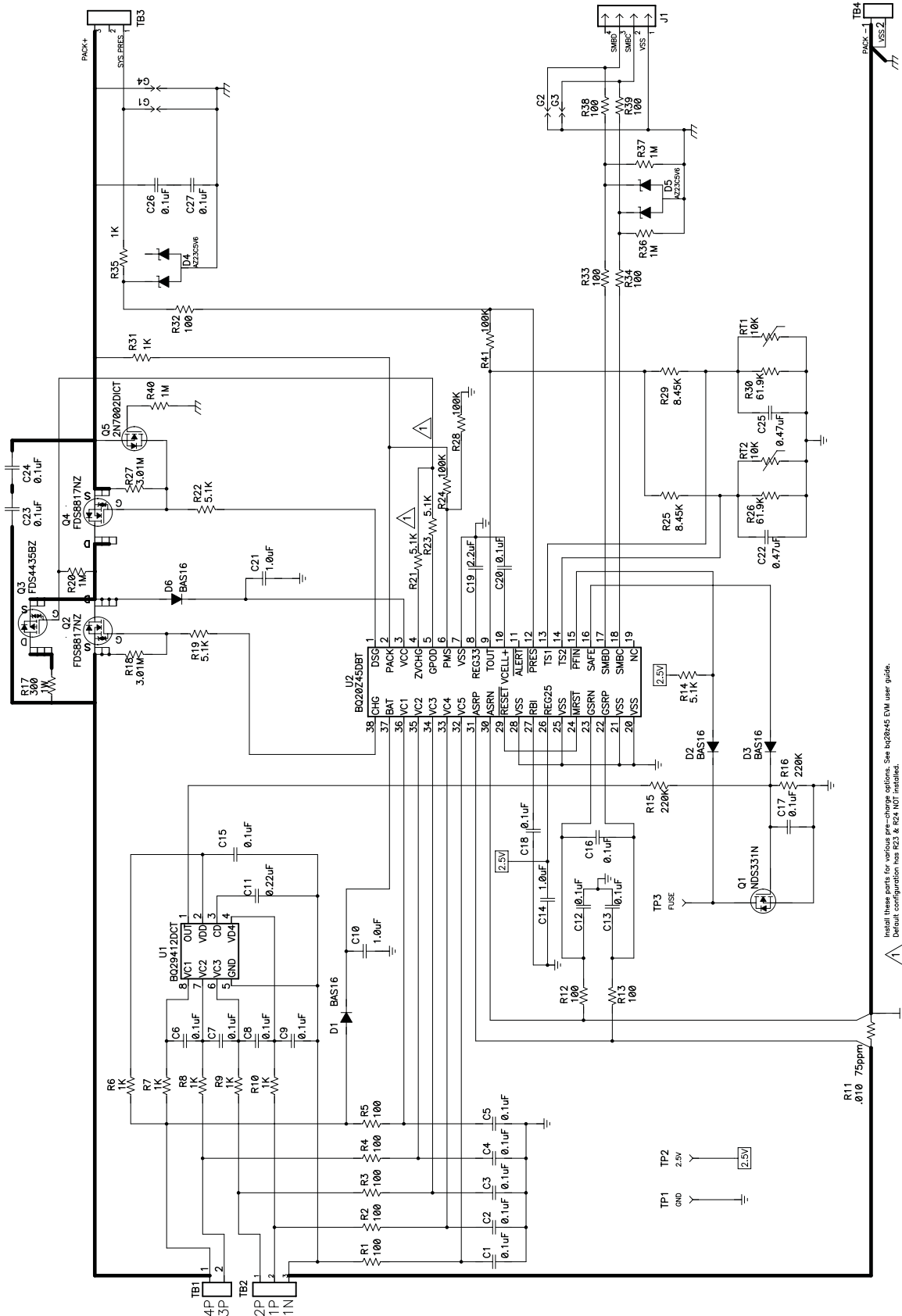
Table 1. SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	hex	2	0x0000	0xffff	—	—
0x01	R/W	RemainingCapacityAlarm	unsigned int	2	0	65535	300	mAh or 10mWh
0x02	R/W	RemainingTimeAlarm	unsigned int	2	0	65535	10	min
0x03	R/W	BatteryMode	hex	2	0x0000	0xe383	—	—
0x04	R/W	AtRate	signed int	2	–32768	32767	—	mA or 10mW
0x05	R	AtRateTimeToFull	unsigned int	2	0	65534	—	min
0x06	R	AtRateTimeToEmpty	unsigned int	2	0	65534	—	min
0x07	R	AtRateOK	unsigned int	2	0	65535	—	—
0x08	R	Temperature	unsigned int	2	0	65535	—	0.1°K
0x09	R	Voltage	unsigned int	2	0	65535	—	mV
0x0a	R	Current	signed int	2	–32768	32767	—	mA
0x0b	R	AverageCurrent	signed int	2	–32768	32767	—	mA
0x0c	R	MaxError	unsigned int	1	0	100	—	%
0x0d	R	RelativeStateOfCharge	unsigned int	1	0	100	—	%
0x0e	R	AbsoluteStateOfCharge	unsigned int	1	0	100+	—	%
0x0f	R/W	RemainingCapacity	unsigned int	2	0	65535	—	mAh or 10mWh
0x10	R	FullChargeCapacity	unsigned int	2	0	65535	—	mAh or 10mWh
0x11	R	RunTimeToEmpty	unsigned int	2	0	65534	—	min
0x12	R	AverageTimeToEmpty	unsigned int	2	0	65534	—	min
0x13	R	AverageTimeToFull	unsigned int	2	0	65534	—	min
0x14	R	ChargingCurrent	unsigned int	2	0	65534	—	mA
0x15	R	ChargingVoltage	unsigned int	2	0	65534	—	mV
0x16	R	BatteryStatus	unsigned int	2	0x0000	0xffff	—	—
0x17	R/W	CycleCount	unsigned int	2	0	65535	—	—
0x18	R/W	DesignCapacity	unsigned int	2	0	65535	4400	mAh or 10mWh
0x19	R/W	DesignVoltage	unsigned int	2	7000	16000	14400	mV
0x1a	R/W	SpecificationInfo	unsigned int	2	0x0000	0xffff	0x0031	—
0x1b	R/W	ManufactureDate	unsigned int	2	0	65535	01-Jan-1980	—
0x1c	R/W	SerialNumber	hex	2	0x0000	0xffff	0x0001	—
0x20	R/W	ManufacturerName	String	20+1	—	—	Texas Inst.	—
0x21	R/W	DeviceName	String	20+1	—	—	bq20z45	—
0x22	R/W	DeviceChemistry	String	4+1	—	—	LION	—
0x23	R	ManufacturerData	String	14+1	—	—	—	—
0x2f	R/W	Authenticate	String	20+1	—	—	—	—
0x3c	R	CellVoltage4	unsigned int	2	0	65535	—	mV
0x3d	R	CellVoltage3	unsigned int	2	0	65535	—	mV
0x3e	R	CellVoltage2	unsigned int	2	0	65535	—	mV
0x3f	R	CellVoltage1	unsigned int	2	0	65535	—	mV

Table 2. EXTENDED SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x45	R	AFEData	String	11+1	—	—	—	—
0x46	R/W	FETControl	hex	2	0x00	0xff	—	—
0x4f	R	StateOfHealth	hex	2	0x0000	0xffff	—	%
0x51	R	SafetyStatus	hex	2	0x0000	0xffff	—	—
0x53	R	PFStatus	hex	2	0x0000	0xffff	—	—
0x54	R	OperationStatus	hex	2	0x0000	0xffff	—	—
0x55	R	ChargingStatus	hex	2	0x0000	0xffff	—	—
0x57	R	ResetData	hex	2	0x0000	0xffff	—	—
0x58	R	WDRResetData	unsigned int	2	0	65535	—	—
0x5a	R	PackVoltage	unsigned int	2	0	65535	—	mV
0x5d	R	AverageVoltage	unsigned int	2	0	65535	—	mV
0x5e	R	TS1Temperature	integer	2	–400	1200	—	0.1°C
0x5f	R	TS2Temperature	integer	2	–400	1200	—	0.1°C
0x60	R/W	UnSealKey	hex	4	0x00000000	0xffffffff	—	—
0x61	R/W	FullAccessKey	hex	4	0x00000000	0xffffffff	—	—
0x62	R/W	PFKey	hex	4	0x00000000	0xffffffff	—	—
0x63	R/W	AuthenKey3	hex	4	0x00000000	0xffffffff	—	—
0x64	R/W	AuthenKey2	hex	4	0x00000000	0xffffffff	—	—
0x65	R/W	AuthenKey1	hex	4	0x00000000	0xffffffff	—	—
0x66	R/W	AuthenKey0	hex	4	0x00000000	0xffffffff	—	—
0x69	R	SafetyStatus2	hex	2	0x0000	0x000f	—	—
0x6b	R	PFStatus2	hex	2	0x0000	0x000f	—	—
0x6c	R/W	ManufBlock1	String	20	—	—	—	—
0x6d	R/W	ManufBlock2	String	20	—	—	—	—
0x6e	R/W	ManufBlock3	String	20	—	—	—	—
0x6f	R/W	ManufBlock4	String	20	—	—	—	—
0x70	R/W	ManufacturerInfo	String	31+1	—	—	—	—
0x71	R/W	SenseResistor	unsigned int	2	0	65535	—	μΩ
0x72	R	TempRange	hex	2	0x0000	0xffff	—	—
0x73	R	LifetimeData	String	32+1	—	—	—	—
0x77	R/W	DataFlashSubClassID	hex	2	0x0000	0xffff	—	—
0x78	R/W	DataFlashSubClassPage1	hex	32	—	—	—	—
0x79	R/W	DataFlashSubClassPage2	hex	32	—	—	—	—
0x7a	R/W	DataFlashSubClassPage3	hex	32	—	—	—	—
0x7b	R/W	DataFlashSubClassPage4	hex	32	—	—	—	—
0x7c	R/W	DataFlashSubClassPage5	hex	32	—	—	—	—
0x7d	R/W	DataFlashSubClassPage6	hex	32	—	—	—	—
0x7e	R/W	DataFlashSubClassPage7	hex	32	—	—	—	—
0x7f	R/W	DataFlashSubClassPage8	hex	32	—	—	—	—

APPLICATION SCHEMATIC



Install these parts for various pre-charge options. See bq20z45 5.1M user guide. Default configuration has R23 & R24 NOT installed.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com