

PCM codec IC for digital cellular telephones

BU8731KV

The BU8731KV is a PCM codec IC developed for use with digital cellular telephones. It contains analog input / output features such as a 14-bit linear precision, μ / A-LAW codec, mic and speaker amplifiers, and switching transistor for the ringer drive. This all makes the BU8731KV perfect for PDC and CDMA-type cellular telephones.

●Applications

Digital cellular telephones

●Features

- 1) +3V single power supply ($V_{DD} = 2.7V$ to $3.3V$).
- 2) Built-in 14-bit precision linear, μ / A-LAW codec.
- 3) Transmission filter for the codec unit conforms to ITU-T recommendations.
- 4) Built-in PLL circuit for system clock generation.
- 5) Clock frequency for PCM data transmission can be set anywhere between 64kHz (128kHz when linear) to 2048kHz.
- 6) Analog input / output functions:
 - Built-in mic amplifier.
 - Built-in receiver speaker amplifier (32 Ω BTL type).
 - Built-in earphone speaker amplifier (32 Ω single type).
- 7) DTMF signal and scale tone signal generator functions are built into the tone signal generator block.
- 8) Internal switching transistor for ringer drive.
- 9) VQFP 48-pin package.
- Built-in drive amplifier for reception REXT (600 Ω).
- Built-in electronic volume control for gain adjustment (for reception, transmission, and tone).
- Data signal I / O circuit allows for connection to external devices.
- For the REXT output and earphone output, soft-mute function reduces pop noise when the power is turned on and off.

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Digital power supply voltage	DV_{DD}	$-0.3 \sim +4.5$	V
Analog power supply voltage	RXV_{DD}	$-0.3 \sim +4.5$	V
	TXV_{DD}	$-0.3 \sim +4.5$	V
Digital input voltage	V_{DIN}	$DV_{SS} - 0.3 \sim DV_{DD} + 0.3$	V
Analog input voltage	V_{AIN}	$RXV_{SS} - 0.3 \sim RXV_{DD} + 0.3$	V
		$TXV_{SS} - 0.3 \sim TXV_{DD} + 0.3$	V
Input current	I_{IN}	$-10 \sim +10$	mA
Power dissipation	P_d	400*1	mW
Operating temperature	T_{stg}	$-50 \sim +125$	$^\circ\text{C}$
Storage temperature	T_{opr}	$-20 \sim +85$	$^\circ\text{C}$

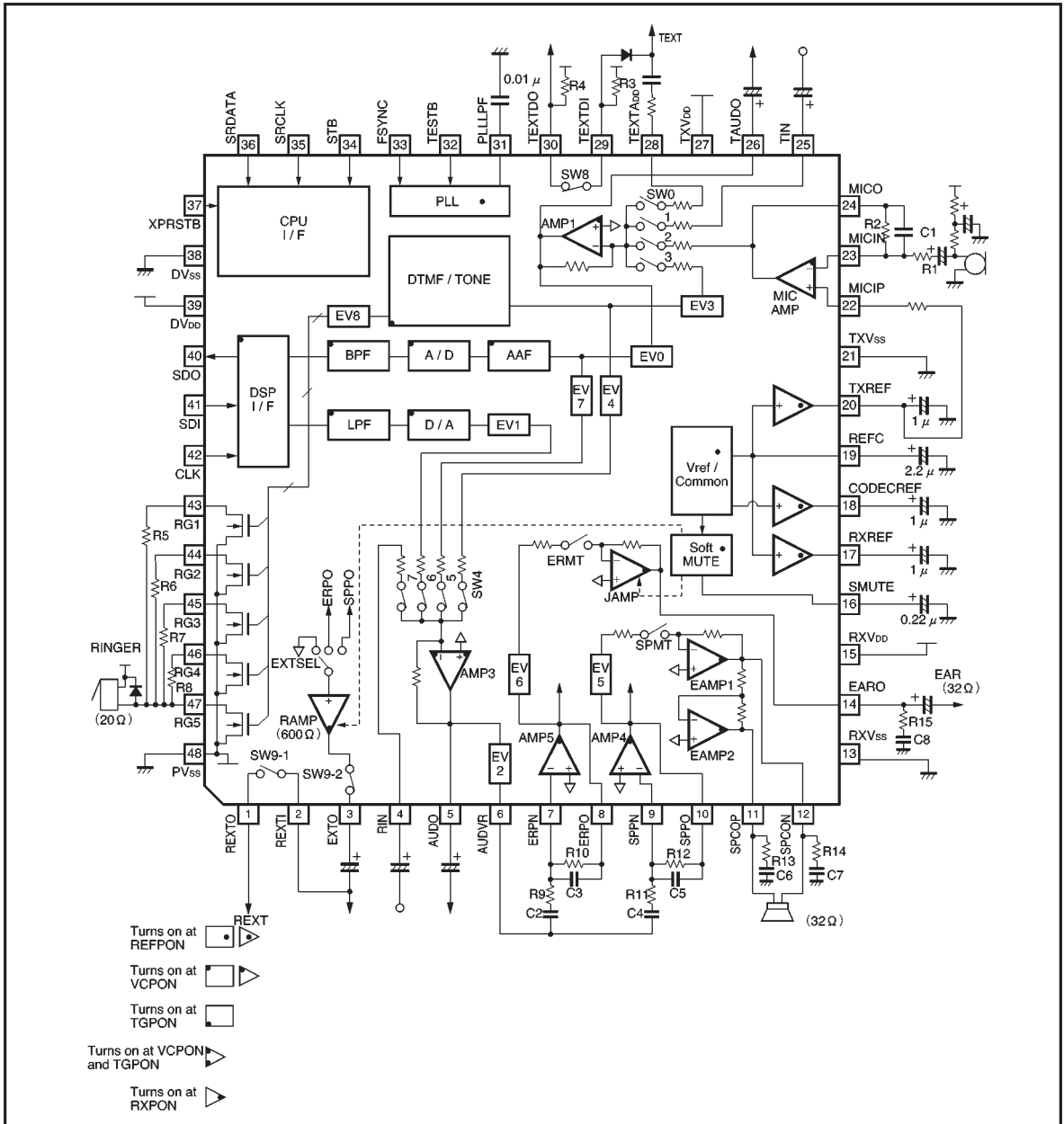
*1 Reduced by 4.0mW for each increase in T_a of 1°C over 25°C .

● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital power supply voltage	DV _{DD}	2.7	—	3.3	V
Analog power supply voltage	RXV _{DD}	2.7	—	3.3	V
	TXV _{DD}	2.7	—	3.3	V

© Not designed for radiation resistance.

● Block diagram



● Pin descriptions

Pin No.	Pin name	I/O	Function	Minimum load resistance (Ω)	Maximum load capacitance (F)
1	REXTO	I/O	Reception data output	—	—
2	REXTI	I/O	Reception data input	—	—
3	EXTO	O	Amplifier output for reception signal gain adjustment	600	—
4	RIN	I	Reception audio direct input	—	—
5	AUDO	O	Reception signal direct output	50k	50p
6	AUDVR	O	Reception signal external output	50k	50p
7	ERPNI	I	Amplifier inverse input for earphone gain adjustment	—	—
8	ERPO	O	Amplifier output for earphone gain adjustment	50k	50p
9	SPPNI	I	Amplifier inverse input for speaker gain adjustment	—	—
10	SPPO	O	Amplifier output for speaker gain adjustment	50k	50p
11	SPCOP	O	Receiver speaker amplifier non-inverse output	32 (BTL)	—
12	SPCON	O	Receiver speaker amplifier inverse output	32 (BTL)	—
13	RXV _{SS}	—	Analog ground for reception	—	—
14	EARO	O	Earphone speaker amplifier output	32	—
15	RXV _{DD}	—	Analog power supply for reception	—	—
16	SMUTE	I	Time constant for soft mute setting	—	0.22 μ *1
17	RXREF	O	Analog reference voltage output for reception	—	1 μ *1
18	CODCREF	O	Analog reference voltage output for codec	—	1 μ *1
19	REFC	O	Analog reference voltage output	—	2.2 μ *1
20	TXREF	O	Analog reference voltage output for transmission	—	1 μ *1
21	TXV _{SS}	—	Analog ground for transmission	—	—
22	MICIP	I	Mic amplifier non-inverse input	—	—
23	MICIN	I	Mic amplifier inverse input	—	—
24	MICO	O	Mic amplifier output	50k	50p
25	TIN	I	Transmission audio direct input	—	—
26	TAUDO	O	Transmission analog output	50k	50p
27	TXV _{DD}	—	Analog power supply for transmission	—	—
28	TEXTA _{DD}	I	Transmission signal incremental input	—	—
29	TEXTDI	I/O	Transmission data signal input	—	—
30	TEXTDO	I/O	Transmission data signal output	—	—
31	PLLLPF	I/O	Input/output filter connector for PLL circuit	—	0.01 μ *1
32	TESTB	I	Test input (\rightarrow DV _{DD})	—	—
33	FSYNC	I	PLL reference clock input	—	—
34	STB	I	CPU I/F strobe input	—	—
35	SRCLK	I	CPU I/F shift clock input	—	—
36	SRDATA	I	CPU I/F address data input	—	—
37	XPRSTB	I	System reset input (L: reset)	—	—
38	DV _{SS}	—	Digital ground	—	—

*1 Recommended value.

Pin No.	Pin name	I / O	Function	Minimum load resistance (Ω)	Maximum load capacitance (F)
39	DV _{DD}	—	Digital power supply	—	—
40	SDO	O	PCM signal output	—	—
41	SDI	I	PCM signal input	—	—
42	CLK	I	PCM signal shift clock input	—	—
43	RG1	O	Ringer drive transistor output 1	100 (for 3V)	—
44	RG2	O	Ringer drive transistor output 2	60 (for 3V)	—
45	RG3	O	Ringer drive transistor output 3	40 (for 3V)	—
46	RG4	O	Ringer drive transistor output 4	30 (for 3V)	—
47	PG5	O	Ringer drive transistor output 5	20 (for 3V)	—
48	PV _{SS}	—	Ground for ringer	—	—

● Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0\text{V}$, $FSYNC = 8\text{kHz}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
〈DC characteristics〉						
Current consumption*1	I_{DD1}	—	8.0	(11.5)	mA	All power on (FSYNC=8kHz)
	I_{DD2}	—	7.0	(10.2)	mA	Reference, audio, SPC on (FSYNC=8kHz)
	I_{DD3}	—	6.0	(8.6)	mA	Reference, audio, earphone on (FSYNC=8kHz)
	I_{DD4}	—	5.4	(7.8)	mA	Reference, audio, RAMP on (FSYNC=8kHz)
	I_{DD5}	—	5.1	(7.3)	mA	Reference and audio on (FSYNC=8kHz)
	I_{DD6}	—	3.7	(5.3)	mA	Reference and tone on (FSYNC=8kHz)
	I_{DD7}	—	3.3	(4.8)	mA	Only reference on (FSYNC=8kHz)
	I_{DD8}	—	0.1	20	μA	Complete power down (FSYNC=fixed)
Digital input high level voltage	V_{IH}	0.8 DV_{DD}	—	—	V	—
Digital input low level voltage	V_{IL}	—	—	0.2 DV_{DD}	V	—
Digital input high level current	I_{IH}	—	—	10	μA	$V_{IH}=DV_{DD}$
Digital input low level current	I_{IL}	-10	—	—	μA	$V_{IL}=0\text{V}$
Digital output high level voltage	V_{OH}	DV_{DD} -0.5	—	—	V	$I_{OH}=-1\text{mA}$
Digital output low level voltage	V_{OL}	—	—	0.5	V	$I_{OL}=1\text{mA}$

*1 The power supply voltage (DV_{DD} , RXV_{DD} , and TXV_{DD}) is 3V. There is no load on the digital and analog output pins.

Digital input pins other than the FSYNC and CLK pins are connected to DV_{DD} or DV_{SS} .

Analog input pins are connected to TXREF or RXREF with the proper resistance.

With soft mute off (SMUTE=0).

- Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0\text{V}$, $FSYNC = 8\text{kHz}$, gain of each attenuator = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		
〈Transmission characteristics〉								
Signal to total power distortion ratio (A→D) TEXTADD→SDO	S_{DT}	24	—	—	dB	1020Hz reference	—45dBm0	C-Wgt
		29	—	—			—40dBm0	
		35	—	—			0~—30dBm0	
Signal to total power distortion ratio (D→A) SDI→AUDO	S_{DR}	24	—	—	dB	1020Hz reference	—45dBm0	C-Wgt
		29	—	—			—40dBm0	
		35	—	—			0~—30dBm0	
Transmission level characteristics (A→D) TEXTADD→SDO	G_{TX}	—0.9	—	0.9	dB	1020Hz reference	—55dBm0	Reference level =—10dBm0 C-Wgt
		—0.6	—	0.6			—50dBm0	
		—0.3	—	0.3			0~—40dBm0	
Transmission level characteristics (D→A) SDI→AUDO	G_{TR}	—0.9	—	0.9	dB	1020Hz reference	—55dBm0	Reference level =—10dBm0 C-Wgt
		—0.6	—	0.6			—50dBm0	
		—0.3	—	0.3			0~—40dBm0	
Transmission output level	V_{OTX}	0.275	0.346	0.436	V_{rms}	1020Hz, 0dBm0 input reference	MICO→SDO	MICO output level is measured
		0.275	0.346	0.436	V_{rms}		TEXTADD →SDO	TEXTADD input level is measured
Reception output level	V_{ORX}	0.291	0.346	0.411	V_{rms}	1020Hz, 0dBm0 input reference	SDI→AUDO	—
Transmission noise during no conversation	V_{NTX}	—	—75	—65	dBm0C	—	MIC→SDO	C-Wgt
Reception noise during no conversation	V_{NRX}	—	—79	—70	dBm0C	—	SDI→AUDO	C-Wgt
Transmission loss frequency characteristics (A→D) TEXTADD→SDO	G_{RX}	24	—	—	dB	1020Hz, 0dBm0 input reference	0.06kHz	—
		0	—	2.5			0.2kHz	
		—0.3	—	0.3			0.3~3.0kHz	
		—0.3	—	0.9			3.4kHz	
		0	—	—			3.6kHz	
		6.5	—	—			3.78kHz	
Transmission loss frequency characteristics (D→A) SDI→AUDO	G_{RR}	—0.3	—	0.3	dB	1020Hz, 0dBm0 input reference	0.0~3.0kHz	—
		—0.3	—	0.9			3.4kHz	
		0	—	—			3.6kHz	
		6.5	—	—			3.78kHz	

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions		
〈Tone generator〉									
Tone output level	HTONE	V_{TNH}	-16	-14	-12	dBV	Set at 2kHz	→AUDIO	30kHz LPF
			-16	-14	-12			→SDO	
	LSTONE	V_{TNL}	-16	-14	-12			→AUDIO	
Tone distortion		S_{DTN}	—	-40	-29	dB	HTONE set at 2kHz	→AUDIO	30kHz LPF
〈Attenuator〉									
Absolute gain	EV0	G_{V0}	10	12	14	dB	MICO→SDO, EV0=12dB		
	EV1	G_{V1}	1	3	5		SDI→AUDIO, EV1=3dB		
	EV2	G_{V2}	-2	0	2		SDI→AUDVR, EV2=0dB		
	EV3	G_{V3}	4	6	8		→SDO, EV3=6dB		
	EV4	G_{V4}	4	6	8		→AUDIO, EV4=6dB		
	EV5	G_{V5}	12	14	16		SPPO→SPCOP-SPCON, EV5=8dB		
	EV6	G_{V6}	6	8	10		ERPO→EARO, EV6=8dB		
	EV7	G_{V7}	-7	-5	-3		MICO→AUDIO, EV7=-5dB		
Volum level setting	EV0	G_{EW0}	-31	—	0	dB	→SDO		
	EV1	G_{EW1}	-7	—	0		→AUDIO		
	EV2	G_{EW2}	-31	—	0		→AUDVR		
	EV3	G_{EW3}	-31	—	0		→SDO		
	EV4	G_{EW4}	-31	—	0		→AUDIO		
	EV5	G_{EW5}	-15	—	0		→SPCOP-SPCON		
	EV6	G_{EW6}	-15	—	0		→EARO		
	EV7	G_{EW7}	-15	—	0		→AUDIO		
Volume step width	EV0	ΔG_{E0}	0.2	1	1.8	dB	→SDO		
	EV1	ΔG_{E1}	0.2	1	1.8		→AUDIO		
	EV2	ΔG_{E2}	0.2	1	1.8		→AUDVR		
	EV3	ΔG_{E3}	0.2	1	1.8		→SDO		
	EV4	ΔG_{E4}	0.2	1	1.8		→AUDIO		
	EV5	ΔG_{E5}	0.2	1	1.8		→SPCOP-SPCON		
	EV6	ΔG_{E6}	0.2	1	1.8		→EARO		
	EV7	ΔG_{E7}	0.2	1	1.8		→AUDIO		

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
〈Mic amplifier〉							
Closed-loop gain	G _{CMC}	0	—	40	dB	→MICO	MIC AMP
〈Reception driver〉							
Closed-loop gain	G _{CAM4}	0	—	40	dB	→SPPO	AMP4
	G _{CAM5}	0	—	40		→ERPO	AMP5
Voltage gain	G _{VRA}	−1.5	0	1.5	dB	→EXTO	RAMP, R _L =600 Ω
Output power	P _{OJA}	2	15	—	mW	→EARO	JAMP, R _L =32 Ω
	P _{OEAE}	6.4	40	—		→SPCOP-SPCON	EAMP2-EAMP1, R _L =32 Ω
Maximum output level	V _{om}	−2	—	—	dBV	→EXTO	RAMP, R _L =600 Ω
〈Ringer drive〉							
Maximum output drive current	I _{O(MAX.)}	150	—	—	mA	VSAT (RG5) <0.7V	
Driven output voltage 1	V _{O1}	—	—	0.7	V	I _o =150mA, RG5	
Driven output voltage 2	V _{O2}	—	—	0.6	V	I _o =100mA, RG4	
Driven output voltage 3	V _{O3}	—	—	0.5	V	I _o =75mA, RG3	
Driven output voltage 4	V _{O4}	—	—	0.4	V	I _o =50mA, RG2	
Driven output voltage 5	V _{O5}	—	—	0.3	V	I _o =30mA, RG1	
OFF leak current	I _L	—	0.1	3	μA	V _o =3V, RG1~RG5=OFF	
〈PLL block〉							
PLL lead-in time	T _{PL}	—	5	(100)	ms	Guaranteed design value	

● Digital AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	
〈Serial data interface / timing〉						
Data clock frequency	μ /A-LAW	f _{CLKU}	64	—	2048	kHz
	Linear	f _{CLKL}	128	—	2048	kHz
Frame sync signal frequency	f _{SYNC}	7.996	8.000	8.004	kHz	
Communication sync signal timing	T _{SR}	100	—	—	ns	
	T _{SS}	100	—	—	ns	
	T _{SH}	100	—	—	ns	
Digital input rise time	T _{IR}	—	—	20	ns	
Digital input fall time	T _{IF}	—	—	20	ns	
SDI setup time	T _{RS}	100	—	—	ns	
SDI hold time	T _{RH}	100	—	—	ns	
〈Register write timing〉						
SRCLK frequency	f _{CLK}	—	—	3	MHz	
SRDATA input setup time	t _{suda}	100	—	—	ns	
SRDATA input hold time	t _{hda}	100	—	—	ns	
Input setup time (SRCLK high vs. STB high)	T _{sud}	333	—	—	ns	
Input hold time (SRCLK high vs. STB low)	t _{hld}	1000	—	—	ns	
STB strobe pulse width	f _{pwd}	667	—	—	ns	

● Measurement circuit

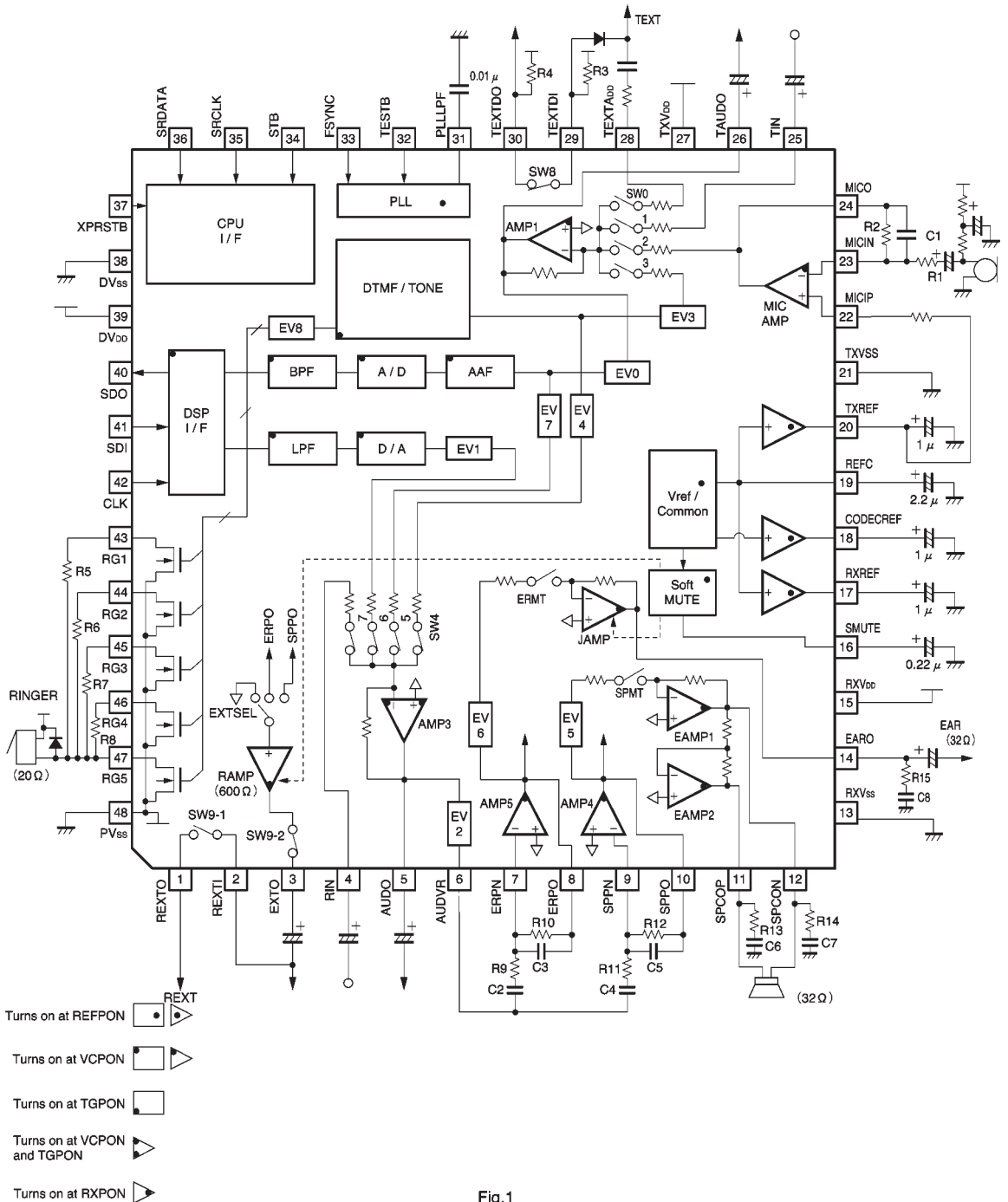


Fig.1

● External dimensions (Units: mm)

