

16-Bit Stereo D/A Converter for Audio applications

BU9480F

The BU9480F is a 16-bit stereo D/A converter designed for audio applications, and has an internal 2× oversampling circuit.

●Applications

16-bit stereo D/A converter for audio applications

●Features

- 1) 3.0 to 5.5V operating voltage.
- 2) Low current consumption because of the CMOS process.
- 3) Resistor string design.
- 4) 2-channel common phase output.
- 5) Internal 2× oversampling interpolator.
- 6) 8-pin plastic package.
- 7) Supports 4fs. (200kHz operation)

●Absolute maximum ratings (Ta=25°C)

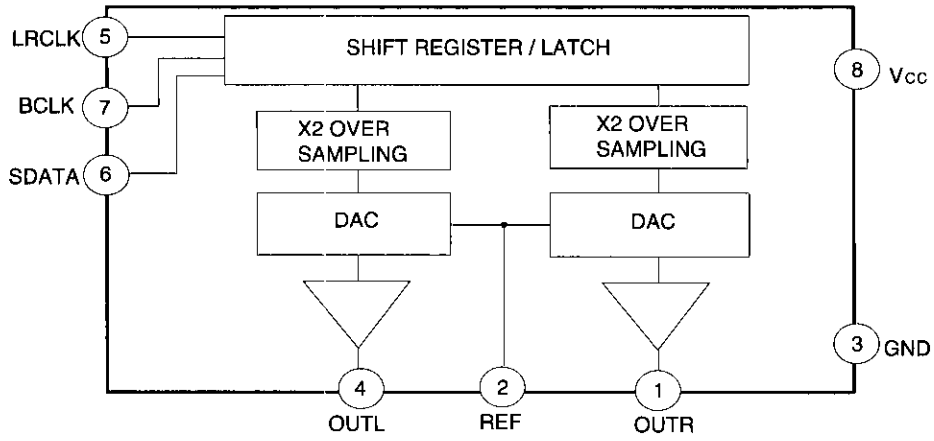
Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DDMax}	7.0	V
Power dissipation	P _d	450*	mW
Operating temperature	T _{opr}	-10~70	°C
Storage temperature	T _{stg}	-55~125	°C
Input voltage	T _{opt}	-0.3~V _{DD} +0.3	V

* When unmounted, reduced by 45 mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	3.0~5.5	V
Input voltage, low level	V _{IL}	0.0~0.2×V _{DD}	V
Input voltage, high level	V _{IH}	0.8×V _{DD} ~V _{DD}	V

●Block diagram



●Pin equivalent circuits

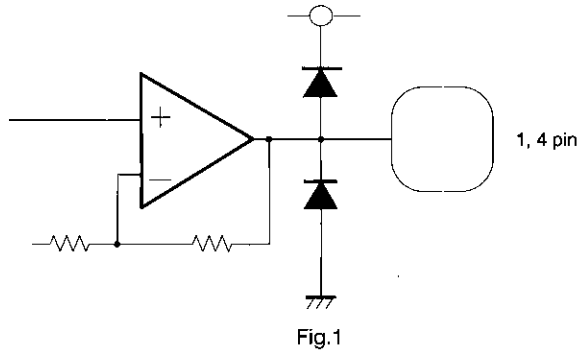


Fig.1

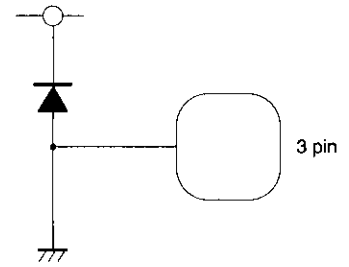


Fig.4

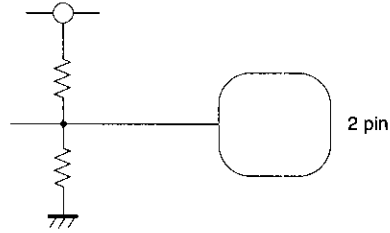


Fig.2

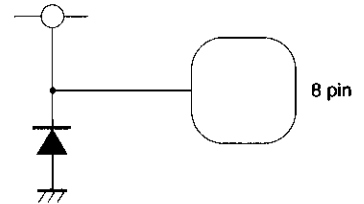


Fig.5

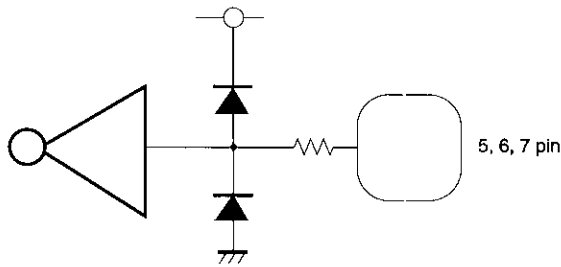


Fig.3

● Pin descriptions

Pin No.	Pin name	Function	I/O	Voltage
1	ROUT	Right channel analog signal output	Low-impedance output	1 / 2V _{CC}
2	REF	Connects the DA ref. voltage pin and ground	High-impedance input	1 / 2V _{CC}
3	GND	Ground	—	—
4	LOUT	Left channel analog signal output	Low-impedance output	1 / 2V _{CC}
5	LRCK	The signal that distinguishes between left and right channels for serial data (left channel = high level, right channel = low level).	Logic input	—
6	SDAT	Serial data input Input with 2' compliment, MSB first.	Logic input	—
7	BCLK	Serial data shift clock input	Logic input	—
8	Vcc	Vcc	—	—

● Electrical characteristics (unless otherwise noted, T_a=25°C, V_{DD}=+5.0V)

Analog unit characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Current consumption	I _{DD}	—	3.6	6	mA	f=1kHz, 0dB	Fig.6,7
Resolution	RES	—	—	16	BIT		Fig.6,7
Noise distortion 1	THD1	—	0.05	0.12	%	f=1kHz, 0dB	Fig.6,7
Noise distortion 2	THD2	—	0.07	0.4	%	f=1kHz, -20dB	Fig.6,7
Full-scale output voltage	V _{FS}	1.8	2	2.2	V _{PP}		Fig.6,7
Crosstalk	C.T	—	-92	-85	dB	Unmeasured channel output = 0 db, f = 1 kHz. DIN audio filter	Fig.6,7
S/N ratio	S / N	86	93	—	dB	DIN audio filter	Fig.6,7
Output pin load resistance	R _L	10	—	—	kΩ		Fig.6,7

Logic input characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Input voltage, high level	V _{IH}	0.7×V _{DD}	—	V _{DD}	V	5,6,7pin	Fig.6,7
Input voltage, low level	V _{IL}	GND	—	0.3×V _{DD}	V	5,6,7pin	Fig.6,7
Leakage current, high level	I _{IH}	—	—	-10	μA	5,6,7pin=V _{DD}	Fig.6,7
Leakage current, low level	I _{IL}	—	—	10	μA	5,6,7pin=GND	Fig.6,7
DA conversion frequency	f _{SL}	—	—	200	kHz		Fig.6,7
BCLK period	T _{BCLK}	60	—	—	nS		Fig.6,7
SDAT.LRCK settling time	T _{ST}	60	—	—	nS		Fig.6,7
SDAT.LRCK holding time	T _{HD}	60	—	—	nS		Fig.6,7

● Measuring circuit

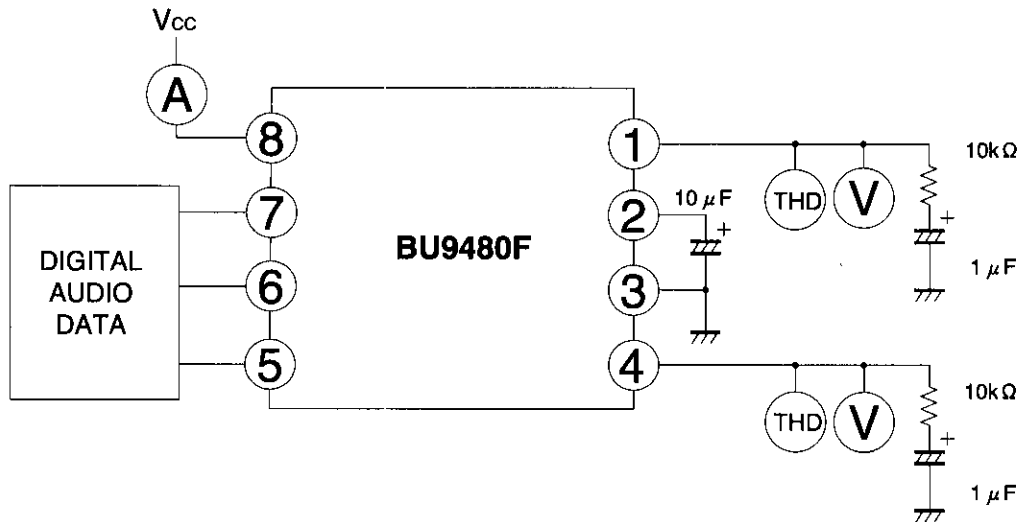


Fig. 6

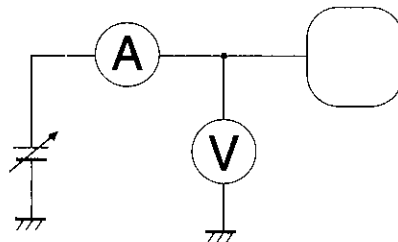
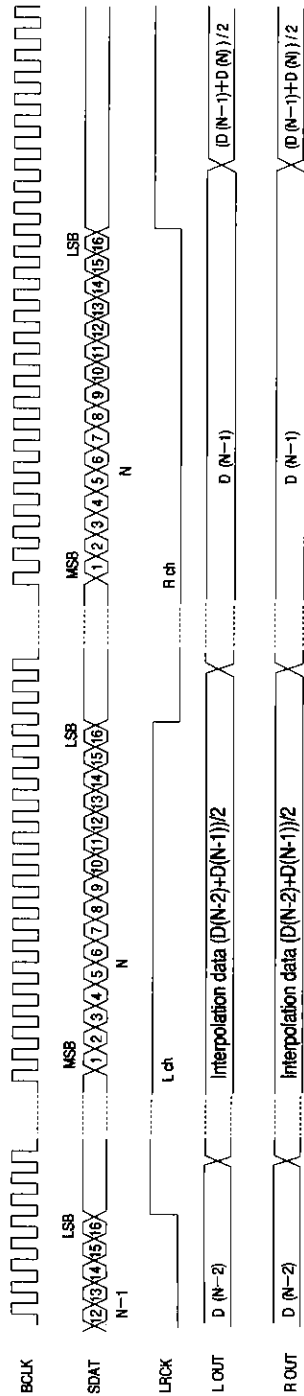


Fig. 7

● I/O signal timing chart



Note: Interpolation and original data output are timed respectively to the leading edge and leading edge of LRCK, and so LRCK should be set to a duty of 50%.

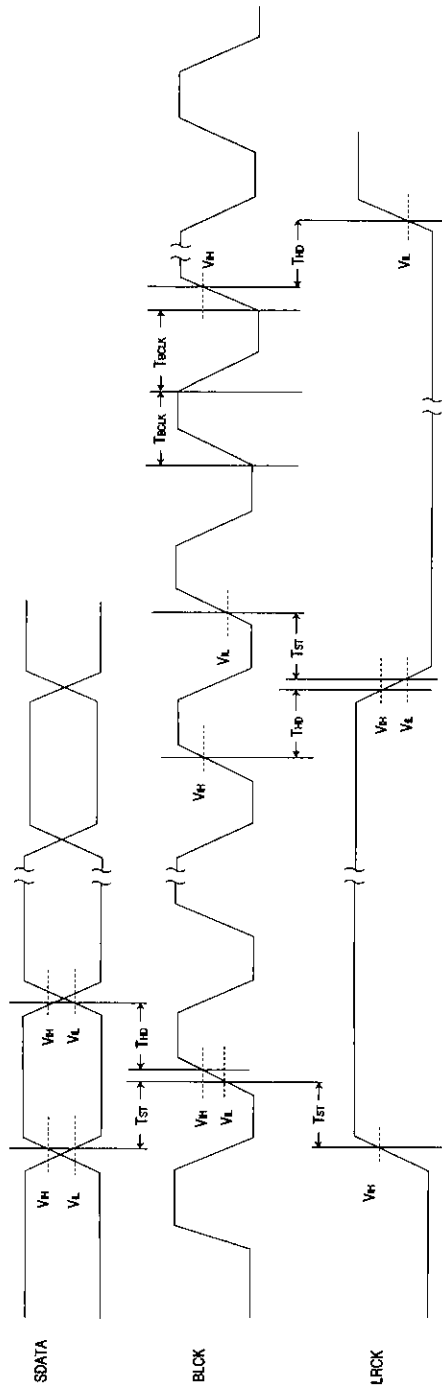
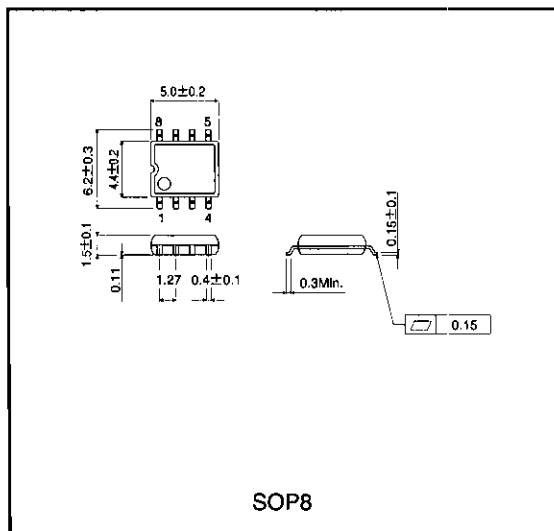


Fig. 8 Measuring circuit

● External dimensions (Units: mm)



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