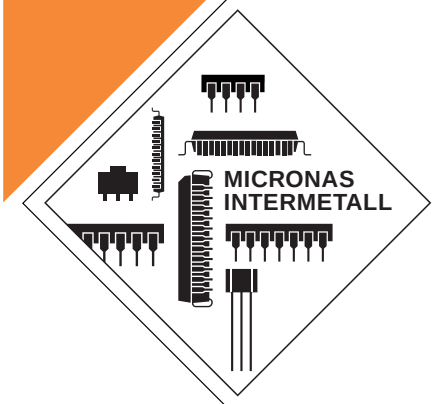

PRELIMINARY DATA SHEET

CAP 3001 A
Car Audio Processor
Hardware

Edition April 4, 1996
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MICRONAS
INTERMETALL

Contents

Contents, continued

Car Audio Processor

1. Introduction

The CAP 3001 A Car Audio Processor presents the one-chip solution for a highly integrated car radio concept. It is housed in a 68-pin Plastic Leaded Chip Carrier Package.

The CAP 3001 A Car Audio Processor is a new CMOS processor to be used for car radio systems.

The application consists essentially of the following components:

– conventional FM tuner, FM–IF stage and FM demodulation

– conventional AM tuner and IF stage

– Car Audio Processor CAP 3001 A

– microcontroller

– analog audio sources

– digital audio source

1.1. Features[1)]

– stereo decoder

– baseband audio processing

– ignition noise canceller

– synthesizer with fast tuning

– AM tuning for 450 to 460 kHz or 10.7 MHz IF

– AM IF processing (450 to 460 kHz)

– AM stereo (C-QUAM) demodulation

– ARI/RDS processing

– PDAI Programmable Digital Audio Interface

– A/D converter

– D/A converter with eightfold oversampling filter.

2. Functional Description

2.1. Architecture

The architecture of the CAP 3001 A processor comprises three main function blocks:

2.1.1. DSP Block

The DSP block consists of a “General Purpose16-Bit Digital Signal Processor” which handles 24 million instructions per second. The data word length is 16 bits and the hardware multiplier operates with an initial word length of $16 \cdot 10$ with a 20-bit result. The memory covers $256 \cdot 16 + 256 \cdot 10$ bit RAM and 2 k instruction ROM.

2.1.2. Digital Part

A main portion consists of hardwired digital filters, such as decimation filters for the A/D converters and interpolation filters for D/A converters. The modulators for ARI/RDS and pilot tone, as well as the complete circuitry for the ignition noise canceller are realized digitally. The logical conclusion for a higher integration is the incorporation of the synthesizer for AM and FM tuning into this hardware block. Naturally the customary serial interfaces for digital audio signals are also included.

2.1.3. Analog Part

In the analog part various input switches, A/D converters and D/A converters are combined. Five A/D converters handle the conversion of analog signals into digital signals. Two of these are specially designed for high quality, one in particular for the conversion of an independent signal path for ARI/RDS signals and the remaining two to be used for the evaluation of analog signals of a lower quality standard (information on field strength and information from potentiometers). Two D/A converters, each equipped with an eightfold oversampling filter, generate analog output signals. These two outputs can be split up and distributed via four independently adjustable volume control switches into four output stages.

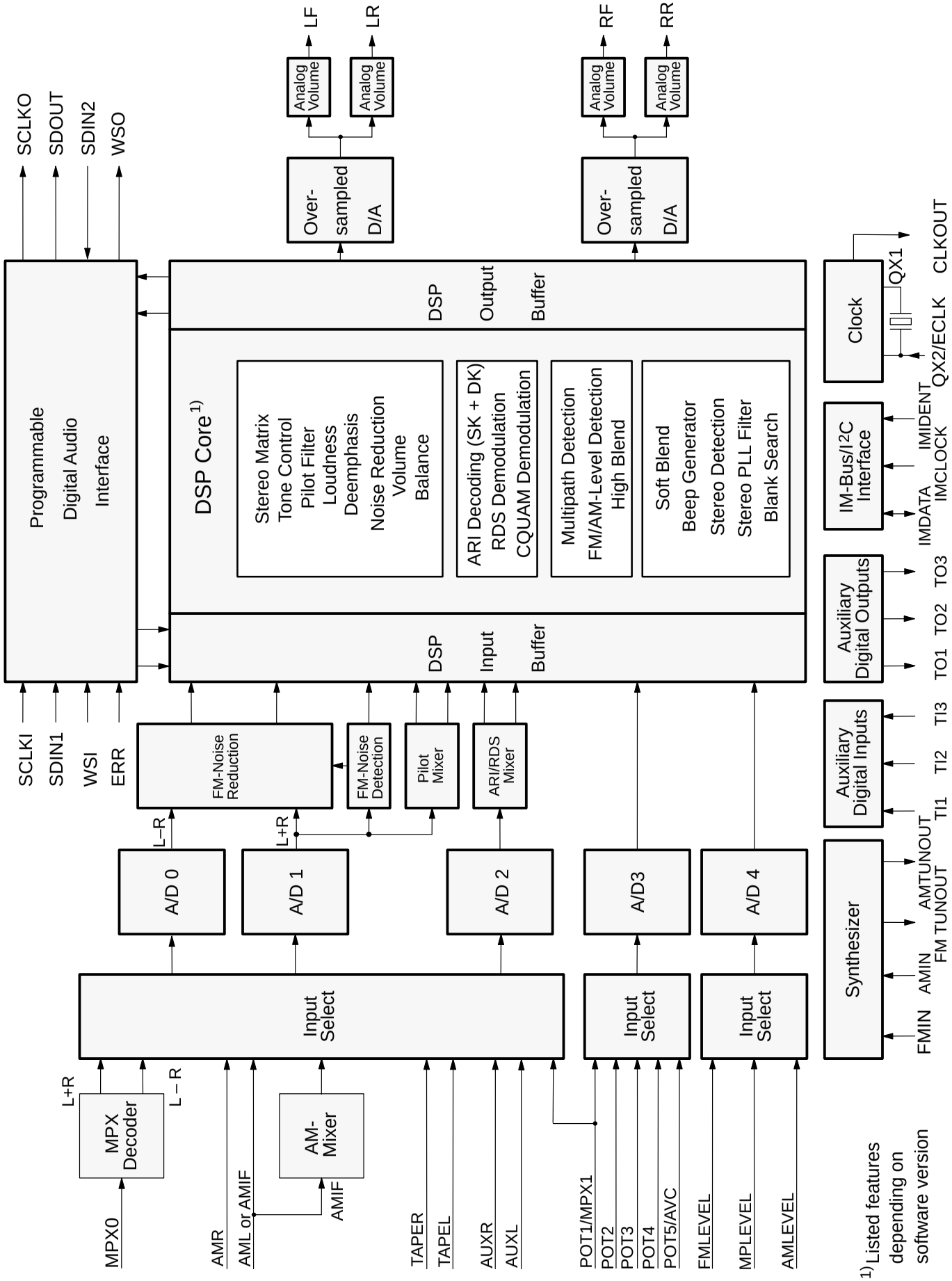


Fig. 2–1: CAP 3001 A block diagram

2.1.4. Operating Modes

The CAP 3001 A possesses 4 main operating modes:

1) MPX-mode

In this mode, the CAP 3001 A receives the multiplex signal of an FM transmission, containing sum and difference channel, the pilot tone and the signals needed for travel information (ARI, RDS). The FM-demodulation has to take place inside the conventional tuner. The mixing of the difference band is done by an analog mixer in front of the A/D-converters in order to achieve the necessary quality for FM stereo. The ARI and RDS signals and the pilot tone are extracted digitally.

2) AF-mode

In this mode the CAP 3001 A works transparently; the incoming signals are only A/D-converted and then transmitted to the DSP core.

3) XDS-mode

In this mode there is an external digital source (XDS, e.g. a CD player) which sends its digital data to the CAP 3001 A for further processing and for the reconverting to analog signals. The CAP 3001 A can be adapted to the sampling rate prescribed by the external digital source; in addition the input systems of the CAP 3001 A remain active in order to monitor the traffic information (ARI/RDS).

4) AM-IF mode

In this mode, the CAP 3001 A receives input signals in the AM-IF range (i.e. 450 to 460 kHz). By a special analog mixer in front of the A/D conversion, the AM signal is mixed down to a frequency of 19 kHz. AM mono and stereo (C-QUAM) are demodulated in the DSP software.

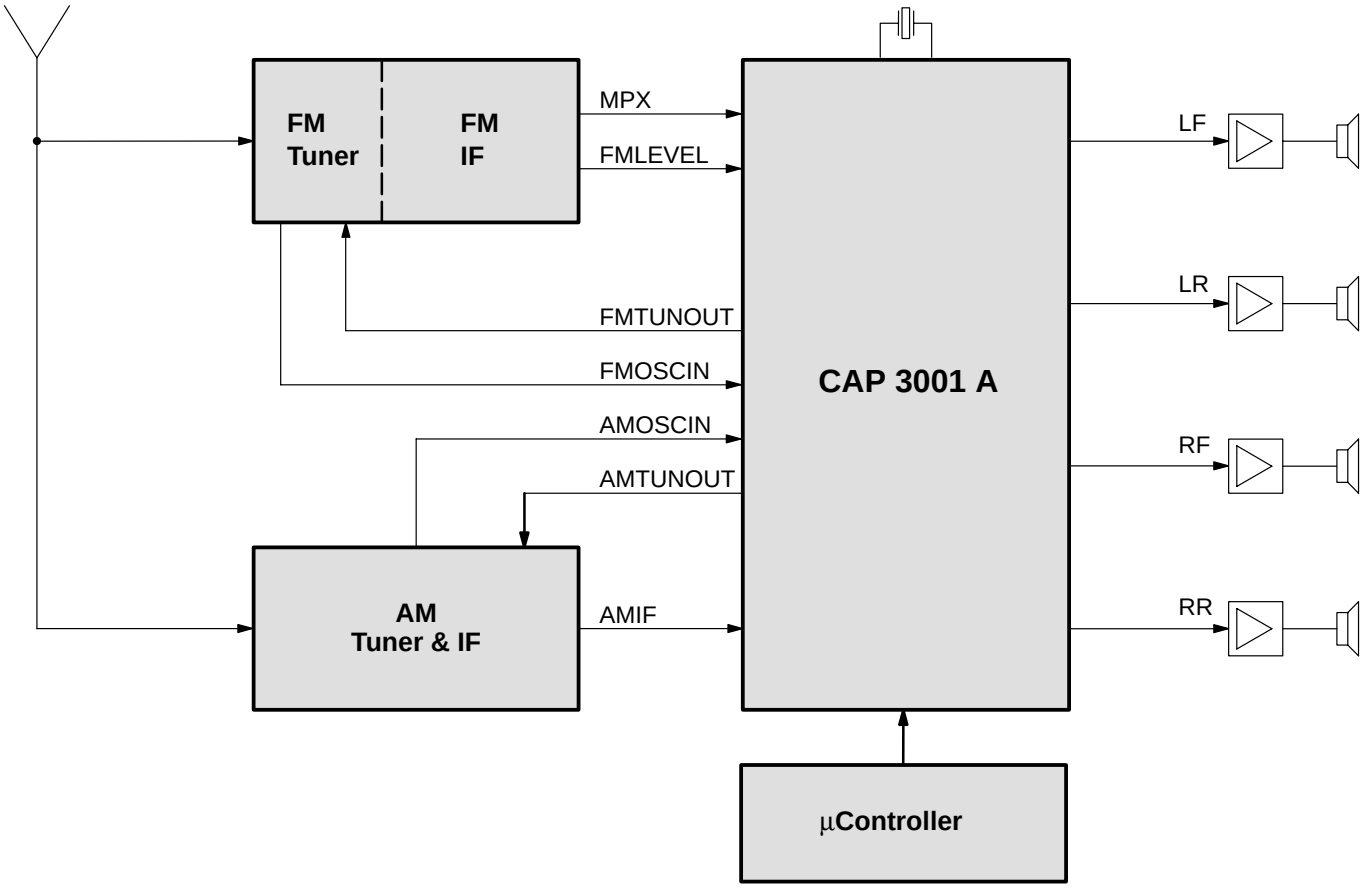


Fig. 2–2: CAP 3001 A system overview

After buffering (ABUF) and switching (AMUX) in the AF-mode the signals are converted into digital form by 2 A/D converters (ADCs). Their output is 1 bit at a rate of 8.208 MHz; in each of the two channels in the CAP 3001 A there is a cascade of 3 lowpass filters (LPF02, LPF23 and LPF34), which suppresses the high-frequency noise produced by the ADCs. The outputs of the filters LPF34 are 16 bits wide and are sampled with 38 kHz; these samples are transmitted via the input buffer to the DSP core. After processing in the DSP, the samples are interpolated to the eightfold sampling rate and converted into analog shape by 2 D/A converters (DACs), filtered (ALPF) and optionally attenuated (AVOL) to feed the power amplifiers which produce the signals for four loudspeakers.

It is assumed that the process of stereo multiplexing used in radio broadcasting is known. The main FM-modulator can be modulated by the sum signal of left and right channel (in baseband), a pilot tone, the difference channel (AM-modulated, suppressed carrier), an optional ARI signal (AM-modulated, unsuppressed carrier) and optionally up to 3 SCA signals (FM-modulated). The composite signal is the so-called MPX signal. So a variety of signals ride “piggy-back” on the main carrier, which was originally assigned only for monophonic transmission. In the CAP 3001 A, the SCA signals are regarded as disturbing signals while the others are regarded as useful.

In the MPX-mode there is an analog mixer AMIX in front of the ADCs. It mixes the difference band down to baseband. The sum channel and the difference channel are then treated like the other baseband signals. Digital quadrature mixers ARIMX and PILMX extract the ARI-information and the information of the pilot signal, respectively.

By means of digital mixers the pilot tone and the ARI signal are mixed down to zero intermediate frequency in quadrature representation, where their information is sampled and sent to the DSP core. The demodulation of the ARI signal is done by the DSP software. The bandwidth of this ARI channel is sufficient to allow demodulation of an RDS (Radio Data System) signal by DSP software as well. Beside these main blocks, there are other systems. The analog field strength information FS delivered by AM and FM tuners is A/D-converted; after lowpass-filtering (LPF06) the samples are sent to the DSP core, where the information could be used to control some parameters of the entire system. Other input signals, such as signals from an external microphone and from external potentiometers are selected by an analog multiplexer, A/D-converted, lowpass-filtered and sent to the DSP or to the controller via the IM-bus interface (IMIF). The IM-bus interface is also able to receive data from the external microcontroller and to control the systems on the CAP 3001 A.

2.1.5. Analog Input Systems

Fig. 2–3 shows all analog inputs and functions of the switches S0 to S3.

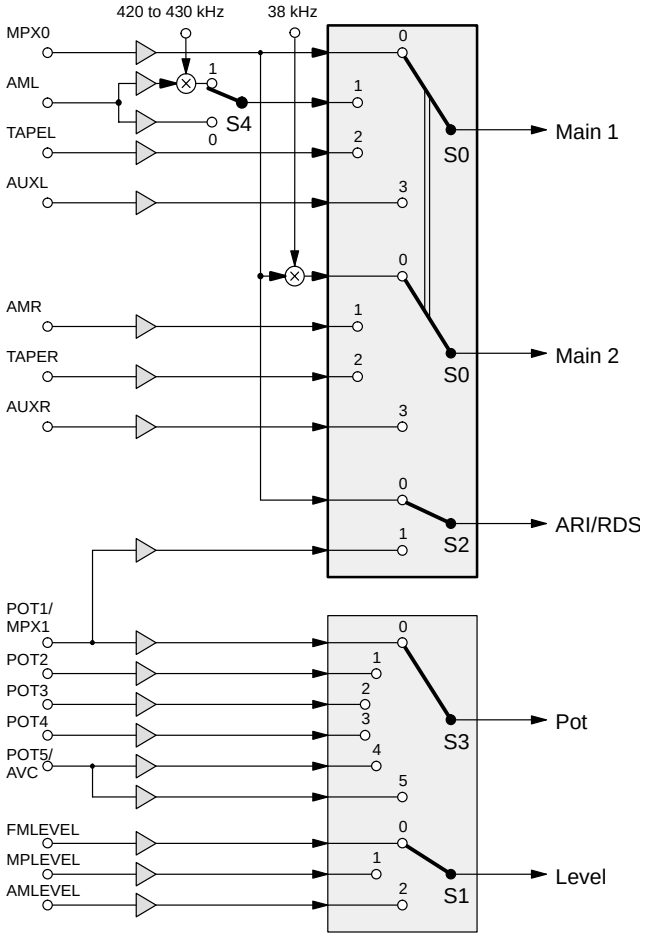


Fig. 2–3: Analog input systems

2.1.6. Buffers ABUF

The analog input buffers have to adjust the individual desired input levels in order to cover the entire volume range of the A/D-converters.

The inputs can be divided into two groups: those which have to be connected via external capacitors, and those that are DC-coupled. One of these inputs, the POT5/AVC-input, uses the same pin, but is DC-coupled if used as POT5, and AC-coupled if used as AVC.

Note: Input pins POT2 to POT5 are switchable to digital outputs via the IM-bus interface. This feature is made possible by open drain transistors and external pull-up resistors down to 1 kΩ.

2.1.7. Stereo Mixer AMIX

This analog demodulator mixes the incoming multiplex signal with the PLL-synchronized 38 kHz subcarrier in order to get the difference channel in baseband.

The phase of the mixer signal is locked to the phase of the digital pilot demodulator; the phase shift between the two signals has to be compensated by the signal processor's Stereo PLL software.

The realized modulator consists of an analog multiplexer switching among the original input signal, the inverted input signal and zero input.

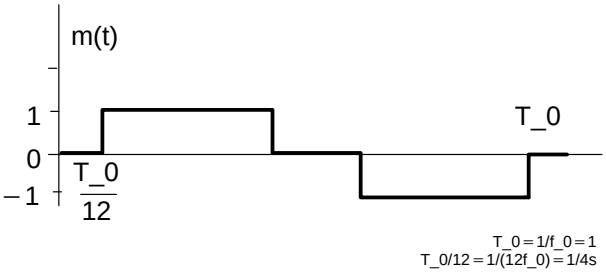


Fig. 2–4: Difference channel mixing signal

The desired fundamental 38 kHz component includes an additional factor of 1.10266 which has to be taken into account in the dematrix-software of the signal processor.

2.1.8. AM Mixer AMMIX

This analog modulator mixes the incoming AM-IF signal down to approximately 19 kHz. Just like the AMIX stereo mixer it uses an amplitude discrete signal instead of a sinusoidal signal.

The realized modulator consists of an analog multiplexer switching among the original input signal and the inverted input signal. The mixing frequency of this mixer is typically between 430 and 440 kHz and can be selected in approximately 2 kHz steps in order to choose the desired AM IF frequency.

2.1.9. Multiplexers AMUX

The analog multiplexers allow the selection of one of the input signals for each signal path.

2.1.10. A/D-Converters ADC

The A/D-converters are realized as pulse density modulators (PDMs) running at a clock frequency of f_s0 = 8.208 MHz. The ADC0, ADC1 and the ADC2 are high quality double-loop PDMs with one external capacitor whereas ADC3 and ADC4 are low quality PDMs without any external capacitor.

2.1.11. Digital Signal Processing Block

2.1.12. Digital Filter Sections

After analog to digital conversion, the input signals are filtered by means of digital filters in order to decimate the high frequency PDM signals to an appropriate sampling rate. The second purpose of these filters is to suppress unwanted out-of-band signals and to shape the input signals to the desired response. After being processed in the DSP section, the digital samples are interpolated to a higher rate before being converted to the analog domain. The individual filter blocks can be seen in Fig. 2–5 and 2–6. Fig. 2–5 shows filter sections for the A/D side whereas in Fig. 2–6, filter blocks for the interpolation process on the D/A side can be seen. In the text of the CAP 3001 A data sheet, the filter blocks are referred to with the names indicated in the schematics.

Most of the filters are designed as multirate FIR blocks. Fig. 2–7 shows the overall (A/D to D/A) passband characteristics of the main channels in TAPE or AUX mode. The shown 3 dB bandwidth is more than 18 kHz. Fig. 2–8 shows the same for the MPX case. An additional pilot notch filter (19 kHz) suppresses higher frequencies. In case of a locked stereo PLL, the suppression is ideal.

Fig. 2–9 depicts the characteristics of the ARI/RDS bandpass. The near-by difference channel is attenuated sufficiently in order to minimize disturbing effects in the weak ARI/RDS signal. An additional lowpass with roll-off characteristics is done in the DSP software.

In order to suppress out-of-band signals, the CAP 3001 A is equipped with digital interpolation filters. These filters attenuate alias frequencies of up to eight times the sampling frequency by at least 50 dB. The interpolation block consists of three cascaded linear phase FIR filters. A simple sample and hold filter serves for the interpolation to the operating rate of the D/A converter. The overall interpolation rate is therefore 32. See Fig. 2–10 for the passband characteristics of the interpolation filter (plotted for 44.1 kHz sampling rate) and Fig. 2–11 for the stopband characteristics.

2.1.13. Digital Mixing Systems

2.1.13.1. Pilot Demodulator PILMX

The entire system is synchronized with the pilot tone of the FM-stereo channel. In the pilot-demodulator 2 mixers working in quadrature are used. The quadrature mixer is the phase detector of the PLL; the other parts of the PLL (loop filter and VCO) are realized in the DSP. The inphase mixer outputs information concerning the level of the pilot tone to the DSP to allow a decision “FM-stereo” or “FM-mono”. The time relation between the mixer sequences of stereo-demodulator and pilot-demodulators is fixed.

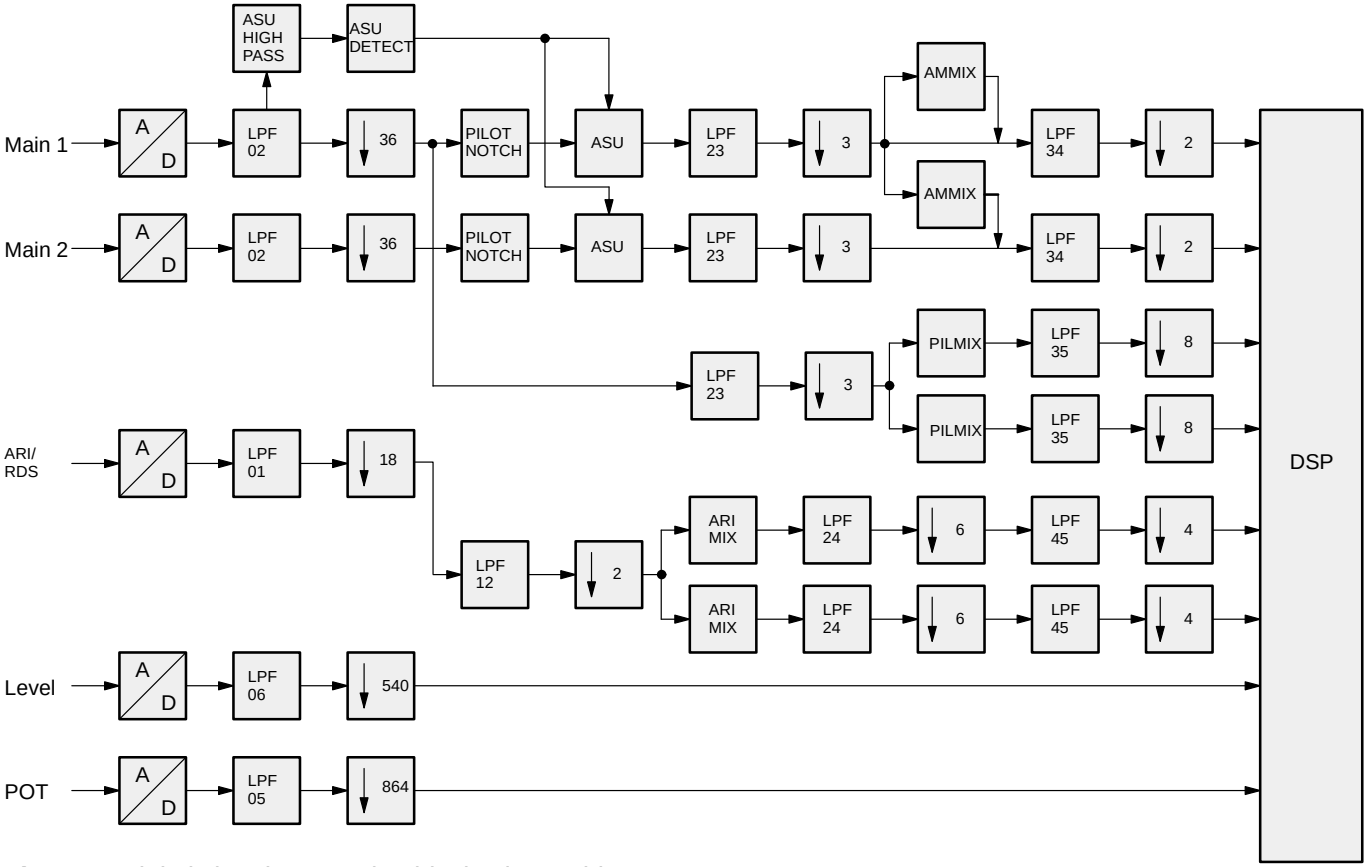


Fig. 2–5: Digital signal processing blocks, input side

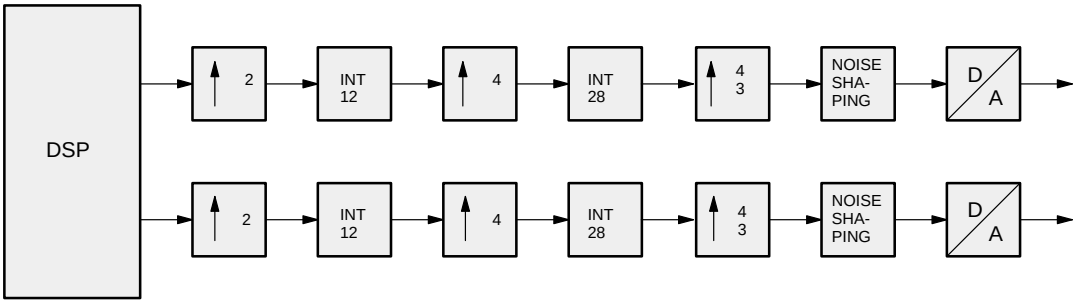


Fig. 2–6: Digital signal processing blocks, output side

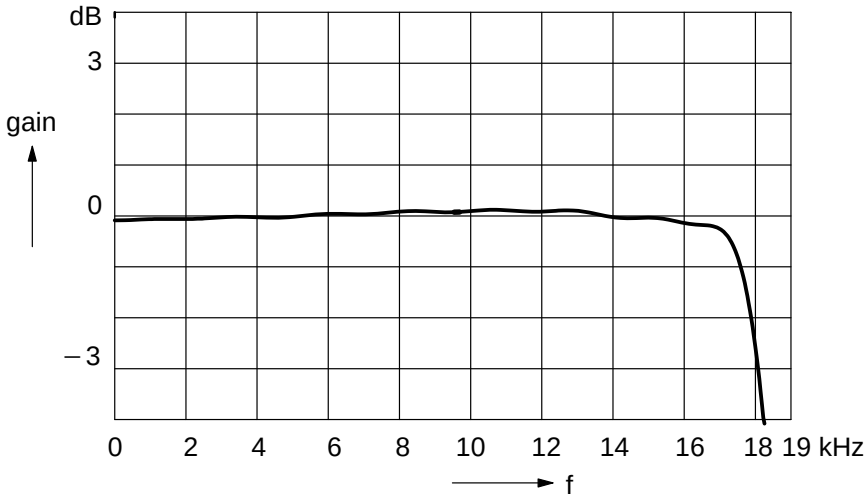


Fig. 2–7: Overall response TAPE/AUX channel

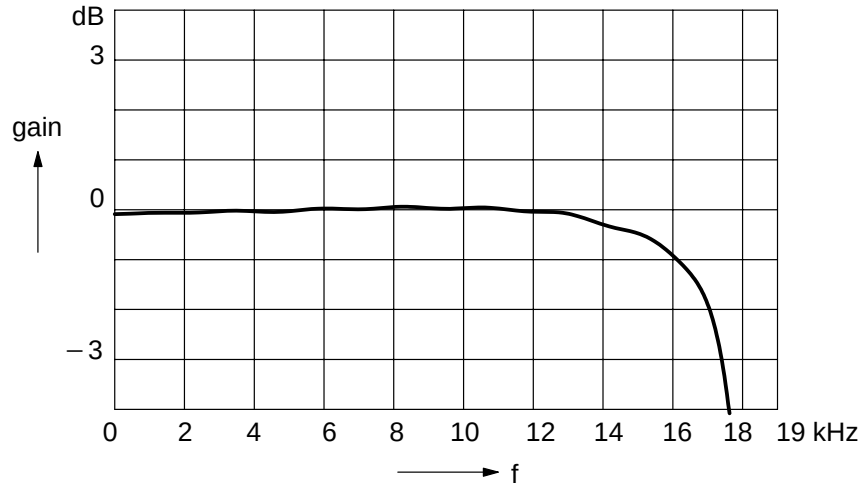


Fig. 2–8: Overall MPX response sum channel

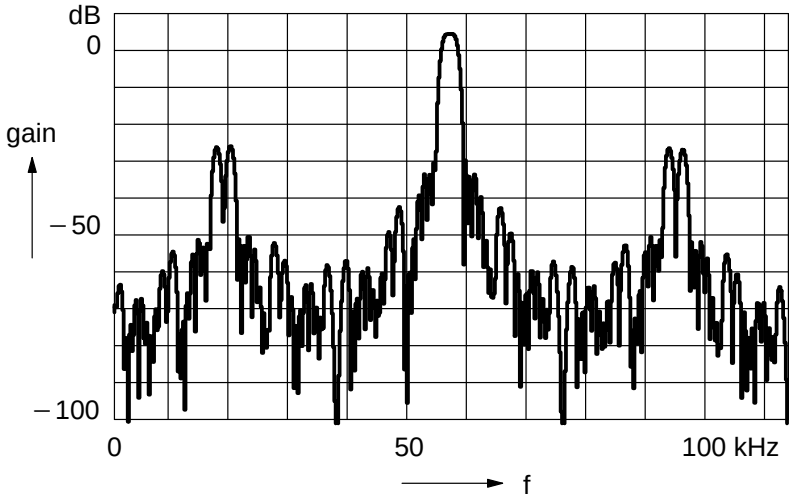


Fig. 2–9: ARI/RDS bandpass characteristic

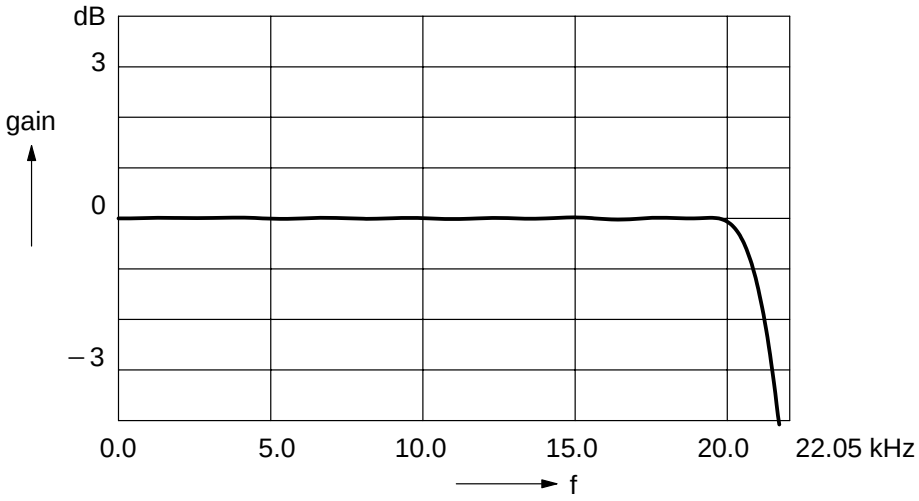


Fig. 2–10: Digital interpolation filter, passband characteristic

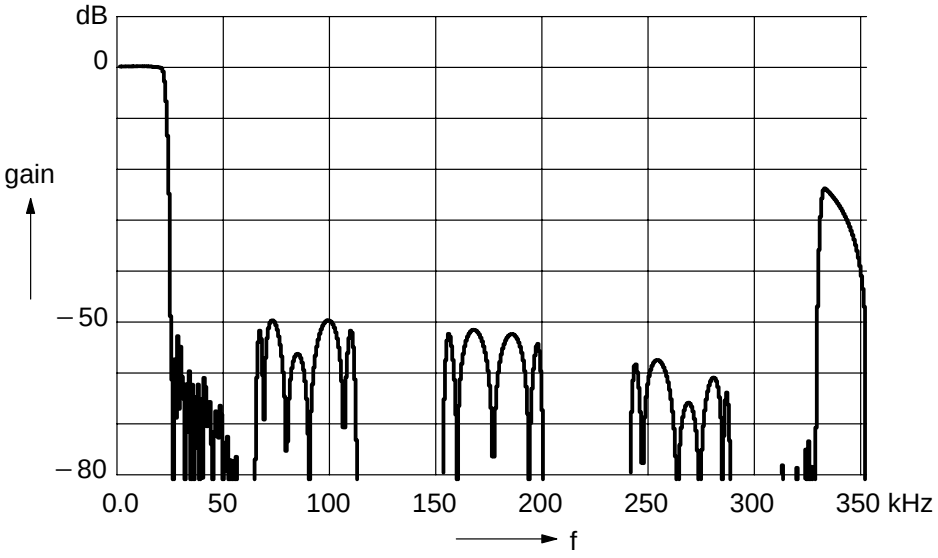


Fig. 2–11: Digital interpolation filter, attenuation

2.1.13.2. ARI Mixer ARIMX

The ARI-information in the range of 57 kHz is mixed down to a zero intermediate frequency by the two ARI mixers, whose mixer signals are again in quadrature. The reason for using two paths is that the demodulation is asynchronous in general; in the DSP there should be an operation which performs the square root of the sum of the squares of the two input signals. The quality requirements of the square rooting should not be very high. Because of the phase lock of pilot tone and ARI carrier in the FM-stereo-mode, a synchronous demodulation seems to be possible; in this case the demodulated ARI signal would be identical with the signal of the inphase path.

The chosen structure has another potential advantage, for processing the radio data system (RDS) in Europe. This signal is a part of the MPX-signal; its subcarrier frequency is the same as that of the ARI-signal but it is recommended that the two subcarriers are in quadrature. So the two paths of the ARI demodulation subsystem make the information of the ARI-signal and of the RDS-signal available to the DSP, where both can be demodulated if desired.

2.1.14. FM Noise Canceller (ASU)

The FM Noise Canceller removes peak noise from the audio signal. No external circuitry is required. All filters, delays and the control section are implemented digitally. The function is split into two sections:

– The noise detection searches for energy in the non-audio range by means of a highpass filter. The output of this filter is compared with a DSP-controlled threshold. If this threshold is exceeded the interpolation unit is triggered. The 19 kHz pilot tone is removed before the audio signal enters the detection highpass. Programmable delay adjustment makes sure of the correct timing between peak detection and peak interpolation.

– The interpolation circuit substitutes a peak-corrupted sample by the mean value of the non-corrupted adjacent samples. Once a trigger comes from the detection circuit, a programmable number (0 to 15) of successive samples is interpolated. All functions work on a 228 kHz sampling rate. At this rate the peaks are still small enough (not widened by the final decimation filters) to be removed effectively.

2.1.15. Analog Output Systems

2.1.16. D/A-Converters DAC

The D/A-converters used are of the oversampling type. The samples to be converted at their sampling rate f_s are first interpolated to 8 x the sampling rate and then oversampled to a higher rate f_NS where noise shaping is performed. The output of the noise shaper is then converted using a highly linear D/A-converter. Its noise power density increases with increasing frequency, the residual noise in the baseband is very low.

Within this application the DAC has to be adapted to the different modes. The digital sources (e.g. CD-player) must supply the proper clock rate in order to drive the DAC with a stable clock rate locked to the sampling rate. The clock is derived from the clock line SCLK of the PDAI bus.

2.1.17. Lowpass-Filters ALPF

The analog lowpass-filters behind the DACs eliminate the high-frequent noise in order to avoid any distortions in the AM frequency range.

2.1.18. Volume Control AVOL

The analog volume control together with the digital volume control implemented in the digital signal processor's software provide a large volume control range. The analog volume control itself covers a range of 45 dB in 1.5 dB steps and includes an additional mute position.

A sensible splitting of the total gain v_tot between the digital gain v_dig and the analog gain v_anlg is:

v_tot	v_anlg	v_dig
$v\_tot \geq 0$ dB	0 dB	v_tot
-45 dB $< v\_tot < 0$ dB	v_tot	0 dB
$v\_tot < -45$ dB	-45 dB	$v\_tot + 45$ dB

All control bits for the hardware section are first addressed to the DSP core program. In case of hardware read-registers the bits are transmitted to the DSP core, stored in the DSP RAM and so they are available for the controller via the DSP's IM-bus interface.

2.1.19. CAP 3001 A - Programmable Digital Audio Interface (PDAI)

The PDAI is the digital audio interface between the CAP 3001 A and external digital sources such as CD/DAT player or additional external processors. It offers a large variety of modes and should therefore cover most of the digital audio standards (I^2S-compatible formats).

Fig. 2–12 shows a standard application with an external digital source and a second CAP 3001 A. The interface is split into the input section and the output section:

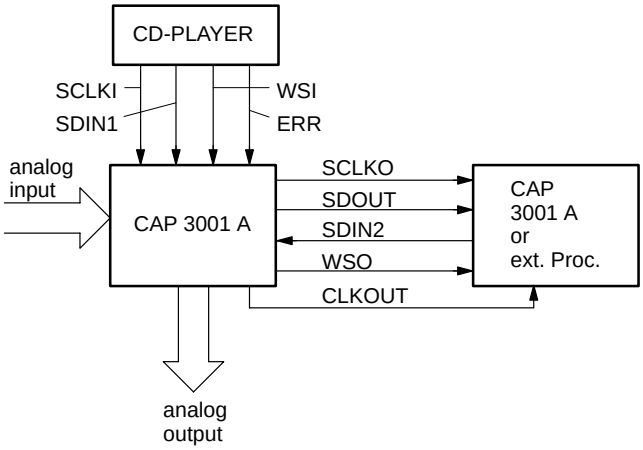


Fig. 2–12: System Configuration

Input Section:

- SCLKI serial clock input
- SDIN1 serial data input 1
- WSI word select input
- ERR error line input

Output Section:

- SCLKO serial clock output
- SDOUT serial data output
- SDIN2 serial data input 2
- WSO word select output

Fig. 2–13 shows the timing of the signals and the programmable features. The programming is done by writing the correct bit patterns into the DSP output buffer. This must be handled by the DSP software.

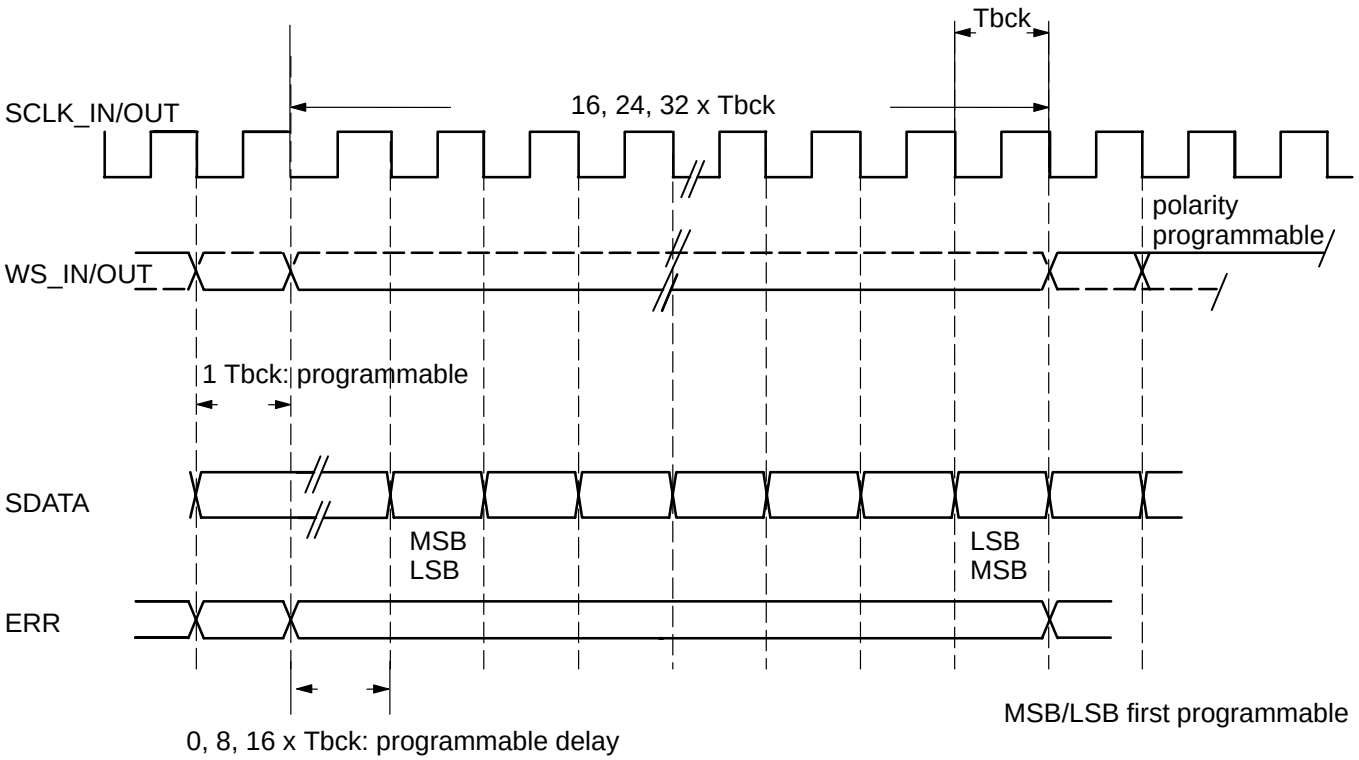


Fig. 2–13: Timing of the signals
Tbck = 1/Fbck

Fbck = 32 · Fsaudio or
Fbck = 48 · Fsaudio or
Fbck = 64 · Fsaudio

The modes are:

– 16-bit wordframe
in this case the programmable delay is set to zero;

– 24-bit wordframe
in this case the programmable delay is set either to 0 or to 8 × Tbck;
this allows left or right adjusted handling of the 16 data bits

– 32-bit wordframe
in this case the programmable delay is set either to 0 or to 16 × Tbck;
this allows left or right adjusted handling of the 16 data bits.

In all modes:

MSB or LSB-first can be selected;
one bit delay between active slope of WSI/O and first wordframe bit is programmable;
the polarity of WSI/O can be programmed ;
in the 24 and 32-bit wordframes the open data bit locations are MSB or LSB extended (depends on left or right adjustment).

Input format and output format can be programmed separately. The restrictions are:

A 24-bit wordframe can only be sent if a 24-bit wordframe is also received. In the analog input mode, the 24-bit wordframe output is not allowed.

2.1.20. The IM Bus Interface of the CAP 3001 A

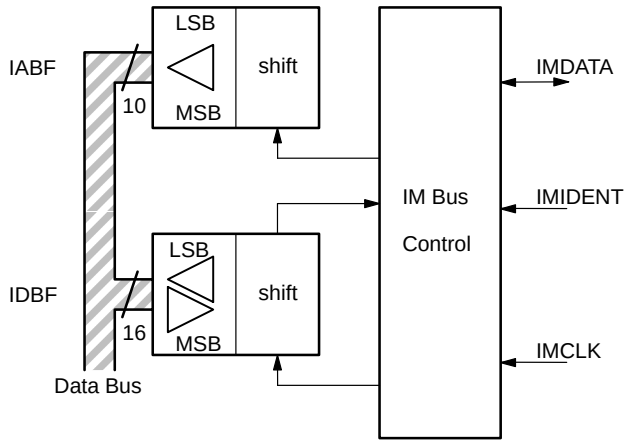


Fig. 2–14: IM-bus interface

The buffer part consists of a unidirectional address buffer IABF with a word length of 10 bit and the bidirectional data buffer IDBF with a word length of 16 bit. It is only possible to write to the address buffer from the peripheral equipment.

By means of the IM-bus interface it is possible, for example, to alter the filter coefficients of the CAP 3001 A. For this purpose the microcomputer writes an address and a data word to the appropriate buffers IABF and IDBF. ***The 10-bit address contains an address part of 8 bits (bit 9 to bit 2), a read/write bit (bit 0) and an additional bit (bit 1) which may be used, for example, for selecting one of the two address counter banks (Fig.*** 2–15***).*** Bits 0 and 1 have the following effect:

ABNK = 0 selects address counter bank 1
ABNK = 1 selects address counter bank 2

R/W = 0 selects Write, microcomputer wants to write
R/W = 1 selects Read, microcomputer wants to read

MSB	Address	LSB	ABNK	R/W

Fig. 2–15: Address format

The following convention is applicable to the data transfer: The last bit written always becomes the MSB of IABF or IDBF. If fewer bits are transferred than the respective buffer size, the unused bits are set to zero in IDBF but remain undefined in IABF. For the output: the first bit output is always the LSB of the IDBF.

2.1.21. Description of the IM Bus

The IM-bus consists of three lines for the signals Ident (IMIDENT), Clock (IMCLK) and Data (IMDATA). The clock frequency range is 50 Hz to 1 MHz. Ident and clock are unidirectional from the controller to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with on-resistances of 150 Ohm maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the controller.

The timing of a complete IM-bus transaction is shown in Fig. 2–16. In the non-operative state the signals of all three bus lines are High. To start a transaction, the controller sets the ID signal to Low level, indicating an address transmission, sets the CL signal to Low level and switches the first bit on the Data line. Then 10 address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM-bus interface switches over to Data read or write, because these functions are correlated to the address.

In the case of a read operation, a fixed wait period has to be observed. This period is defined by the IM-bus handler in the DSP software. For practical reasons this part of the program does not run at the full sampling rate. It is recommended to place the IM-bus handler in a “low speed” time slice in order to save processing power.

For a write operation this wait period does not have to be observed, but please note that the maximum rate of IM-bus transmissions is normally limited by the DSP software.

Also controlled by the address the controller now transmits sixteen clock pulses, and accordingly two Bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data. A bus transaction may be interrupted for up to 10 ms.

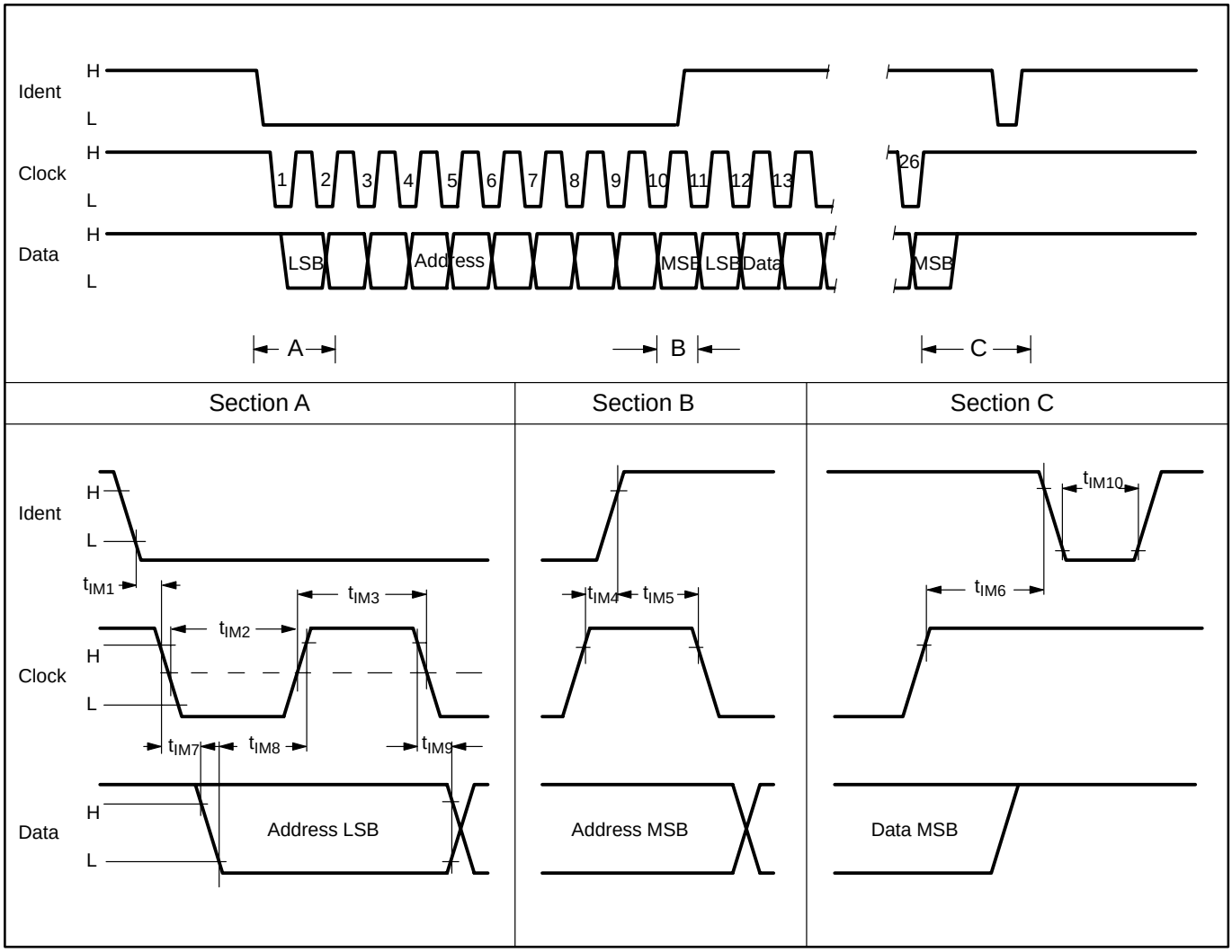


Fig. 2–16: IM Bus waveforms

2.1.22. Clock Generation

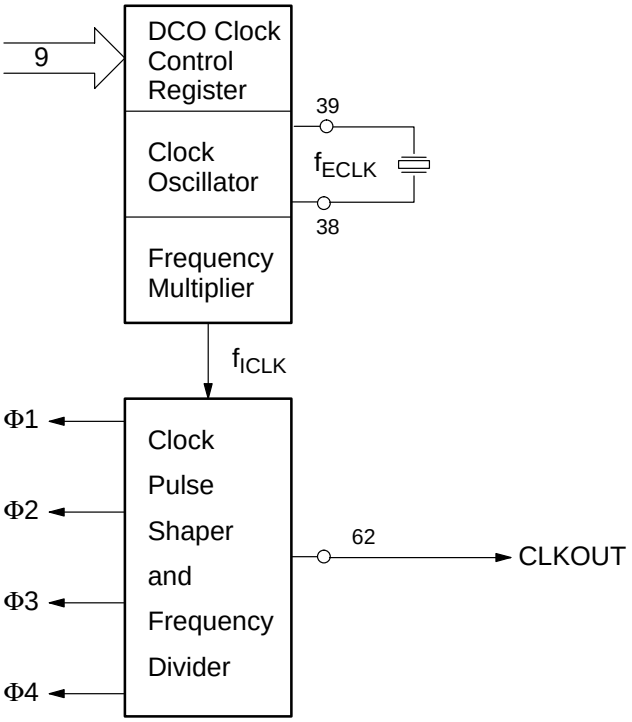
The CAP 3001 A processor has an integrated clock oscillator which is crystal-controlled and oscillates with the frequency $f_{ECLK} = 16.416$ MHz. All components of the oscillator are integrated except for the quartz crystal. This is connected to the QX1 and QX2 oscillator pins. The crystal input QX2/ECLK can be used to supply the CAP 3001 A externally with the required clock. In this case no crystal is needed.

Following the clock oscillator is a frequency multiplier with a factor of 3. The output of the frequency multiplier delivers the f_{ICLK} internal clock frequency, by which the DSP Core is clocked.

There is the possibility of pulling the f_{ECLK} oscillator frequency in a range of 350 ppm, depending on the application and the used crystal. This makes it possible to synchronize the CAP 3001 A to the incoming pilot tone signal in the case of MPX reception.

Table 2–1: Oscillator characteristics

DCO Content	Frequency
011111111B	$f_{ECLKmin}$
000000000B	f_{ECLK}
100000000B	$f_{ECLKmax}$



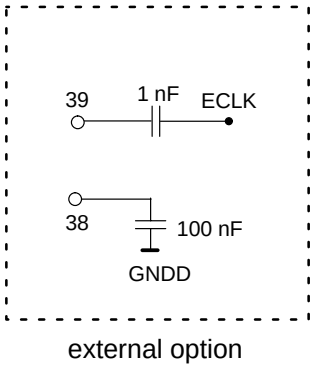


Fig. 2–17: Clock generator connections

3. Specifications

3.1. Outline Dimensions

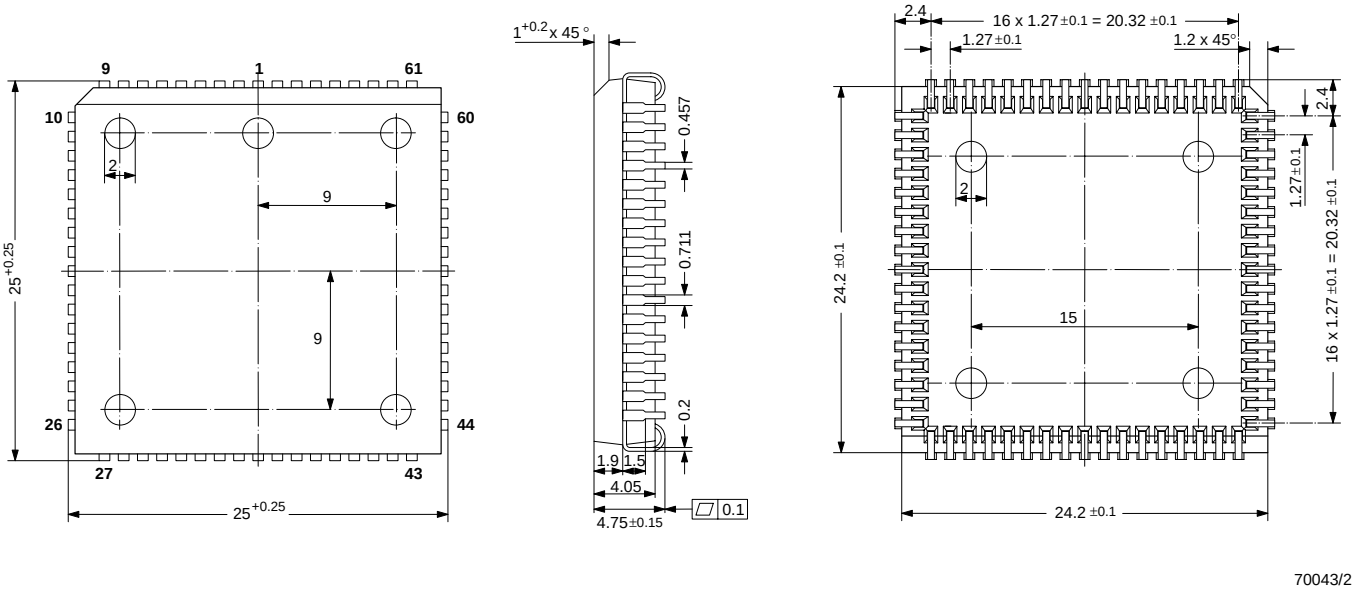


Fig. 3–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm

3.1.1. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
S.T.B. = shorted to BAGNDI if not used
DVSS = if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS = connect to AHVSS

Pin No. PLCC 68-pin	Connection (if not used)	Pin Name	Type	Short Description
1	GNDA	FMLEVEL	IN	FM fieldstrength input
2	GNDA	POT5/AVC	IN/OUT	DC voltage input
3	GNDA	POT4	IN/OUT	DC voltage input
4	GNDA	POT3	IN/OUT	DC voltage input
5	GNDA	POT2	IN/OUT	DC voltage input
6	GNDA	POT1/MPX1	IN/OUT	DC voltage input
7	AGNDC	MPX0	IN	FM MPX signal input
8	AGNDC	AML	IN	AM left baseband input
9	BAGNDC	AMR	IN	AM right baseband input
10	BAGNDC	AUXR	IN	Auxiliary audio input right
11	BAGNDC	AUXL	IN	Auxiliary audio input left
12	BAGNDC	TAPER	IN	Analog tape input right

Pin Connections and Short Descriptions, continued

Pin No. PLCC 68-pin	Connection (if not used)	Pin Name	Type	Short Description
13	BAGNDC	TAPEL	IN	Analog Tape input left
14	BAGNDC	PDMC3	EXT	PDM capacitor connection
15	BAGNDC	PDMC2	EXT	PDM capacitor connection
16	BAGNDC	PDMC1	EXT	PDM capacitor connection
17	LV	BAGNDC	OUT	Buffered internal ground
18	X	AGNDC	EXT	Internal analog ground
19	X	VREF1	IN	Analog ground reference
20	X	GNDA	SUPPLY	Analog ground
21	X	VSUPA	SUPPLY	Analog supply voltage
22	LV	LF	OUT	Analog output left front
23	LV	LR	OUT	Analog output left rear
24	LV	RR	OUT	Analog output right rear
25	LV	RF	OUT	Analog output right front
26	X	VREF2	IN	Analog ground reference synthesizer
27	LV	FMTUNOUT	OUT	FM tuning voltage output
28	LV	TUNFB	IN	Tuning voltage feedback input
29	LV	AMTUNOUT	OUT	AM tuning voltage output
30	VREF2	VSUP2	SUPPLY	Analog supply voltage synthesizer
31	VREF2	VSUP1	SUPPLY	Analog supply voltage synthesizer
32	LV	AMOSCREF	EXT	AMOSC capacitor connection
33	LV	AMOSCIN	IN	AM oscillator signal input
34	LV	FMOSCREF	EXT	FMOSC capacitor connection
35	LV	FMOSCIN	IN	FM oscillator signal input
36	X	GNDS1	SUPPLY	Analog ground synthesizer
37	GNDD	TESTEN	IN	Test Mode Enable
38	X	QX1	IN	Crystal
39	X	QX2/ECLK	IN	Crystal/External clock input
40	X	RESET	IN	Reset input
41	X	IMDATA	IN/OUT	IM-bus/I^2C data input/output
42	X	IMCLK	IN	IM-bus/I^2C clock input

Pin Connections and Short Descriptions, continued

Pin No. PLCC 68-pin	Connection (if not used)	Pin Name	Type	Short Description
43	X	IMIDENT	IN	IM-bus ident input
44	GNDD	TEOSC	IN	Test purpose
45	LV	REFCLK	IN	Synthesizer Ref. Frequency input
46	LV[1)]	TI1	IN	Static digital input 1
47	LV[1)]	TI2	IN	Static digital input 2
48	LV[1)]	TI3	IN	Static digital input 3
49	LV	SCLKO	OUT	Serial clock output
50	LV	WSO	OUT	Serial word select output
51	LV	SDOUT	OUT	Serial data output
52	LV	SDIN2	IN	Serial data input 2
53	LV	ERR	IN	Serial error input
54	LV	SCLKI	IN	Serial clock input
55	LV	WSI	IN	Serial word select input
56	LV	SDIN1	IN	Serial data input 1
57	LV	TO1	OUT	Digital output 1
58	LV	TO2	OUT	Digital output 2
59	LV	TO3	OUT	Digital output 3
60	X	GNDD	SUPPLY	Digital ground
61	X	VSUPD	SUPPLY	Digital supply voltage
62	LV	CLKOUT	OUT	Clock output
63	GNDD	TP3	IN	Test purpose
64	LV	TP2	OUT	Test purpose
65	LV	TP4	OUT	Test purpose
66	GNDD	TP1	IN	Test purpose
67	GNDA	AMLEVEL	IN	AM fieldstrength input
68	GNDA	MPLEVEL	IN	Multipath signal input

[1)] Depending on software version.

3.1.2. Pin Descriptions

Pin1 – FMLEVEL
Input for the FM field strength information.

Pins 2 to 6 – POT5/AVC, POT4, POT3, POT2, POT1/MPX1
Inputs for a DC-control voltage (0V to V_{SUP}). These pins can also be used as digital outputs with an external pull-up resistor; the function and selection is controlled via IM/I^2C-bus.
POT1/MPX1 also serves as a second MPX input for ARI/RDS.
POT5/AVC also serves as a highly sensitive microphone input.

Pin 7 – MPX0
Input for the MPX signal in case of FM reception.

Pin 8 – AML
Input for left channel baseband audio; or for AM IF (450 to 460 kHz).

Pin 9 – AMR
Input for right channel baseband audio.

Pin 10 – AUXR
Input for additional audio sources, right channel.

Pin 11 – AUXL
Input for additional audio sources, left channel.

Pin 12 – TAPER
Input for right tape channel.

Pin 13 – TAPEL
Input for left tape channel.

Pins 14 to 16 – PDMC3, PDMC2, PDMC1
Capacitor pins for the feedback loop of the high quality pulse-density modulators.

Pin 17 – BAGNDC
Buffered internal ground. This pin is the buffered internal ground connection for the external PDM capacitors.

Pin 18 – AGNDC
This pin serves as internal ground connection for the analog circuitry. It must be connected to analog ground with a 4.7 µF and a 100 nF capacitor in parallel.

Pin 19 – VREF1
This pin must be connected separately to the single ground point. It serves as ground connection for the analog bias circuits.

Pin 20 – GNDA
This pin serves as ground connection for the analog signals and NF parts of the synthesizer section.

Pin 21 – VSUPA
Analog supply voltage; power for the analog circuitry of the CAP 3001 A is supplied via this pin.

Pin 22 – LF
Left front speaker output.

Pin 23 – LR
Left rear speaker output.

Pin 24 – RR
Right rear speaker output.

Pin 25 – RF
Right front speaker output.

Pin 26 – VREF2
This pin serves as ground connection for the synthesizer bias circuits and must be connected separately to the ground point of the tuner.

Pin 27 – FMTUNOUT
Tuning voltage for the FM oscillator.

Pin 28 – TUNFB
Feedback input for tuning voltage amplifier.

Pin 29 – AMTUNOUT
Tuning voltage for the AM oscillator.

Pin 30 – VSUP2
Synthesizer supply voltage 2; power is supplied via this pin for the synthesizer output circuitry of the CAP 3001 A.

Pin 31 – VSUP1
Synthesizer supply voltage 1; power is supplied via this pin for the synthesizer circuitry of the CAP 3001 A.

Pin 32 – AMOSCREF
Capacitor pin for AMOSCIN reference voltage.

Pin 33 – AMOSCIN
Input for the AM oscillator signal.

Pin 34 – FMOSCREF
Capacitor pin for FMOSCIN reference voltage.

Pin 35 – FMOSCIN
Input for the FM oscillator signal.

Pin 36 – GNDS1
This pin serves as ground connection for the HF parts of the synthesizer section.

Pin 37 – TESTEN
Test mode enable

Pin 38 – QX1
Crystal pin. This pin has to be connected with the crystal.

Pin 39 – QX2/ECLK
Crystal pin. This pin has to be connected with the crystal or with an external clock signal.

Pin 40 – RESET
In the steady state, high level is required at this pin. A low level resets the CAP 3001 A.

Pins 41 to 43 – IMDATA, IMCLK, IMIDENT
Via these pins the CAP 3001 A sends and receives data to and from the controller.

Pin 44 – TEOSC
Test purpose.

Pin 45 – REFCLK
Input for the synthesizer reference frequency.

Pins 46 to 48 – TI1, TI2, TI3
Static digital inputs; these signals can be used as a branch condition in the DSP software. If not used, they must be connected to GND.

Pin 49 – SCLKO
DAI-Bus: serial clock output.

Pin 50 – WSO
DAI-Bus: word select output; this is a control line to separated left and right channel in the serial DAI stream.

Pin 51 – SDOUT
DAI-Bus: serial data output.

Pin 52 – SDIN2
DAI-Bus: serial data input 2.

Pin 53 – ERR
DAI-Bus: error input.

Pin 54 – SCLKI
DAI-Bus: serial clock input.

Pin 55 – WSI
DAI-Bus: word select input; this is a control line to separate left and right channel in the serial DAI stream.

Pin 56 – SDIN1
DAI-Bus: serial data input 1.

Pins 57 to 59 – TO1, TO2, TO3
Digital outputs; the logical state can be defined by the DSP software.

Pin 60 – GNDD
This pin serves as ground connection for the digital signals.

Pin 61 – VSUPD
Digital supply voltage. Power is supplied via this pin for the digital circuitry of the CAP 3001 A.

Pin 62 – CLKOUT
This output is used for clocking external hardware.

Pin 63 – TP3
Test purpose.

Pin 64 – TP2
Test purpose.

Pin 65 – TP4
Test purpose.

Pin 66 – TP1
Test purpose.

Pin 67 – AMLEVEL
Input for the AM field strength information.

Pin 68 – MPLEVEL
Input for the multipath information.

3.1.3. Pin Configuration

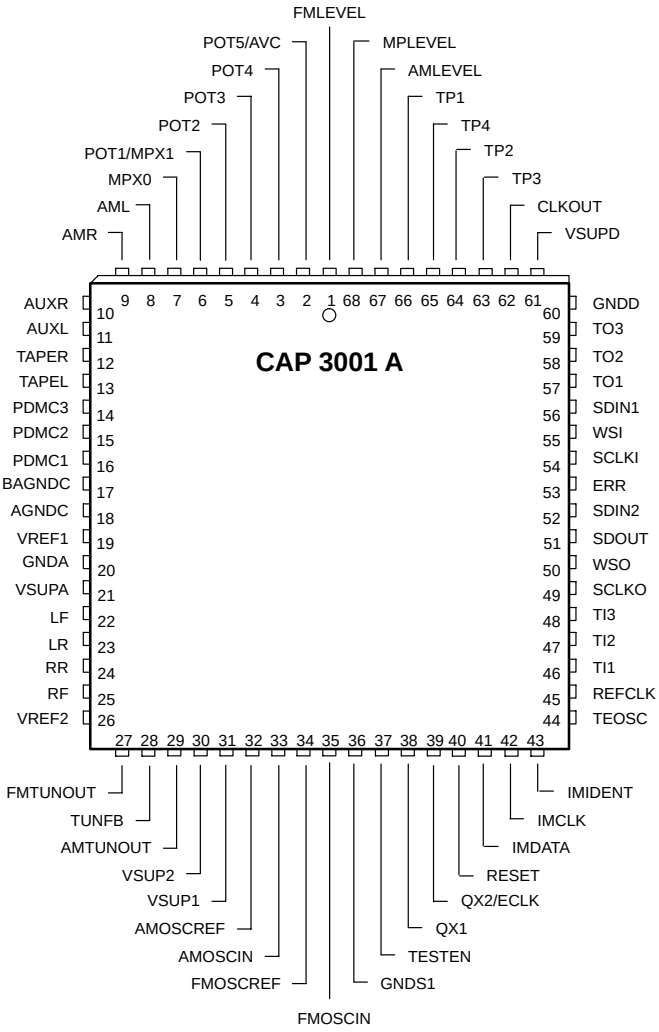


Fig. 3–2: Pinning of the CAP 3001 A in PLCC68 package, top view

3.1.4. Electrical Characteristics

All voltages refer to ground.

3.1.5. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	−20	+85	°C
T_S	Storage Temperature	–	−55	+125	°C
V_{SUP}	Supply Voltage	21, 61	−0.3 [1)]	+6	V
V_{SUP1}	Supply Voltage	31	−0.3 [1)]	+6	V
V_{SUP2}	Supply Voltage	30	−0.3 [1)]	+12	V
P_{TOT}	Chip Power Dissipation 68-pin PLCC without heatspreader	21, 61, 30, 31	–	1300	mW
dV_{SUP}	Voltage between VSUPA, VSUPD and VSUP1	21, 61, 31	− 0.5	+ 0.5	V
V_I	Input Voltage, all Inputs	1 to 17, 28, 32 to 35, 38, 39, 41 to 48, 52 to 56, 67, 68	−0.3	V_{SUP} +0.3	V
I_O	Output Current, all Outputs	22 to 25, 27, 29, 41, 49 to 51, 57 to 59, 62	–	[2)] [3)]	–

[1)] Reversed supply 200 ms maximum.
[2)] The outputs are short-circuit proof (max. 5 seconds) with respect to supply and ground.
[3)] Total chip power dissipation must not exceed absolute maximum ratings.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions/Characteristics of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.1.6. Recommended Operating Conditions at $T_A = -20$ to $+85$ °C, $f_{ECLK} = 16.416$ MHz, typical values at $T_j = 27$ °C, duty cycle = 50 %

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	21, 61	4.75	5.0	5.25	V
V_{SUP1}	Supply Voltage	31	4.75	5.0	5.25	V
V_{SUP2}	Supply Voltage	30	7.5	8.5	9.5	V

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{ECLKL}	ECLK Clock Input Low Voltage	39	–	–	1.5	V
V_{ECLKH}	ECLK Clock Input High Voltage		V_{SUP} −1.5	–	–	V
$\frac{t_{ECLKH}}{t_{ECLKL}}$	ECLK Clock Input High/Low Ratio		0.9	1.0	1.1	–
f_{ECLK}	ECLK Clock Input Frequency (see also chapter 3.1.7.)		–	16.416	–	MHz
$V_{REFCLKH}$	Reference Clock Input High Voltage	45	V_{SUPD} –1.5	–	–	V
$V_{REFCLKL}$	Reference Clock Input Low Voltage		–	–	1.5	V
$V_{REFCLK0}$	Reference Clock Input Open Circuit Voltage			$\frac{V_{SUP}}{2}$		–
f_{REFCLK}	Refence Clock Input Frequency		1		16	MHz
V_{FS}	DC Input Voltage FM, AM, MP level	1, 67, 68	0		V_{SUP}	–
$V_{POT/MPXI}$	DC Input Voltage POT5, POT4, POT3, POT2, POT1 (with $I \leq 20$ mA)	2 to 6	0		V_{SUP}	–
V_{IH}	High Level, Digital Inputs	46 to 50, 52 to 56	2.0			V
V_{IL}	Low Level, Digital Inputs				0.8	V
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	40	–	–	0.8	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		V_{SUP}– 0.8V	–	–	–
V_{IMIL}	IM Bus Input Low Voltage	41 to 43	–	–	1.5	V
V_{IMIH}	IM Bus Input High Voltage		3.0	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	1000	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		0.5	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		0.5	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5} write data	ΦI Clock Input Hold Time after Ident Input High		0.25	–	–	µs
t_{IM5} read data	ΦI Clock Input Hold Time after Ident Input High		defined by DSP software			µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End-Pulse Input	41 to 43	1.0	–	–	µs

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM7}	IM Bus Data Input Delay after ΦI Time Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time		1.0	–	–	µs
C_{PDM}	PDM Capacitor (Low Loss Type)	14 to 16	−5%	680	+5%	pF
C_{AGNDC}	AGNDC-Filter-Capacitor	18		3.3		µF
	Ceramic Capacitor in parallel			100		nF
f_{SCLKI}	Input SCLKI Frequency	54	–	–	3.1	MHz
t_{SIJ}	Input SCLKI Phase Jitter		–	–	250	ps
t_{SIW}	Input SCLKI Pulse Width		40	50	60	%
t_{IDS}	Input Data Setup Time	56, 52	40	–	–	ns
t_{IDH}	Input Data Hold Time		0	–	–	–
t_{WSS}	Input WSI Setup Time Output WSO Setup Time	50, 55	40	–	–	ns
t_{WSH}	Input WSI Hold Time Output WSO Hold Time		0	–	–	–

3.1.7. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	−20	–	+85	°C
f_P	Parallel Resonance Frequency	–	16.416[1)]	–	MHz
$\frac{\Delta f_S}{f_S}$	Accuracy of Adjustment	–	–	±20	ppm
$\frac{\Delta f_S}{f_S}$	Frequency Deviation versus Temperature	–	–	±40	ppm
R_r	Series Resistance	–	–	15	Ω
C_0	Shunt Capacitance	5.5	–	7	pF
C_1	Motional Capacitance	25	30	–	fF
df	Frequency pulling range	350	–	–	ppm

[1)] at $C_L = 10.7$ pF.

Remark on defining the external load capacitance: External capacitors at each crystal pin to ground are required. The higher the capacity, the lower the clock frequency results. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application.

3.1.8. Characteristics at $T_A = -20$ to $+85$ °C, V_{SUP} and $V_{SUP1} = 4.75$ to 5.25 V, $V_{SUP2} = 7.5$ to 9.5 V, $f_{ECLK} = 16.416$ MHz, typical values at V_{SUP} and $V_{SUP1} = 5.0$ V, $V_{SUP2} = 8.5$ V, $T_j = 27$°C and duty cycle = 50 %.

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
Z_{AII1}	Analog Input Impedance ($f_{signal} = 1$kHz, $i = 10$ µA) AVC, MPX1, MPX0, AM, AUX, TAPE at $T_j = 27$°C at $T_j = -20$ to $+85$ °C	2, 6 to 13	 27 26	 35	 43 47	 kΩ
Z_{AII2}	Analog Input Impedance FM, AM, MP level	1, 67, 68		200		kΩ
Z_{POT}	Analog Input Impedance POT1...5	2 to 6		200		kΩ
V_{OSCI0}	Open Circuit Voltage FMOSCIN, AMOSCIN	33, 35		$\frac{V_{SUP1}}{2}$		–
R_{OPOT}	Output Resistance POT1 to 5 as outputs, $i \leq 5$ mA	2 to 6		80		Ω
R_{OSCI}	Analog Input Resistance FMOSCIN, AMOSCIN, FMOSCREF, AMOSCREF at $T_j = +27$ °C at $T_j = -20$ to $+85$ °C	33, 35	 3.2 2.1	 3.6 3.6 4	 4.2 6.5	 kΩ kΩ pF
R_{AO}	Analog Output Resistance LF, LR, RR, RF ($f_{signal} = 1$kHz, $i = 1$ mA) at $T_j = 27$°C, at $T_j = -20$ to $+85$ °C	22 to 25	 470 440	 600	 730 790	 Ω
$V_{MPX0/1I}$	Input Voltage MPX0, MPX1	7, 6			2.0	V_{PP}
$V_{AML/RI}$	Input Voltage AML, AMR	8, 9			1.1	V_{RMS}
$V_{TAPER/TAPELI}$	Input Voltage TAPER, TAPEL	12, 13			1.6	V_{RMS}
$V_{AUXR/LI}$	Input Voltage AUXR, AUXL	10, 11			1.1	V_{RMS}
V_{AVCI}	Input Voltage AVC	2			0.007	V_{RMS}
V_{AICL}	Analog Audio Input Clipping Level (defines 0 dBr)	6 to 13	Max. Input Voltage	Max. Input Voltage +1 dB	Max. Input Voltage + 2 dB	
Z_{AOL}	Analog Output Load	22 to 25	6 0.005		 1	kΩ nF
V_{AOV}	Maximum Analog Output Voltage LF, LR, RR, RF (output attenuation = 0 dB, analog output load > 100 kΩ) Analog Input Digital Input	22 to 25	 0.8 0.9	 0.9 1.0	 1.0 1.1	 V_{RMS}
V_{AMOSC}	AM OSC Input Voltage	33	40		300	mV_{RMS}
f_{AMOSCI}	AM OSC Input Frequency Range		0.5		20	MHz

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{FMOSCI}	FM OSC Input Voltage	35	40		300	mV_{RMS}
f_{FMOSCI}	FM OSC Input Frequency Range		60		150	MHz
SNR_{AD}	SNR A/D (Noise measurement RMS unweighted, BW = 20 to 18000 Hz, input level = − 20 dBr, f_{signal} = 1kHz)	7 to 13	82	85		dB
SNR_{DA}	SNR D/A Analog Attenuation = 0 dB Analog Attenuation = 45 dB in MUTE position (RMS, unweighted, BW = 20 to 20000 Hz[1)], input level = − 20 dBFS, f_{signal} = 1kHz)	22 to 25	 90 60	 95 65 110		 dB dB dB
SNR_{RDS1}	SNR A/D selected MPX ARI/RDS channel (Noise measurement RMS, unweighted, BW = 55 to 59 kHz, input level = 55 mV_{PP} f_{signal} = 57 kHz)	6, 7		38		dB
THD_{AD}	THD A/D (RMS, unweighted, BW = 20 to 18000, input level = − 3 dBr, f_{signal} = 1 kHz)	7 to 13			0.03	%
THD_{DA}	THD D/A (BW = 20 to 20000 Hz[1)], input level = − 3 dBFS, f_{signal} = 1kHz, analog attenuation = 0 dB)	22 to 25			0.01	%
IMD_{AD}	Intermodulation Distortion A/D (f_{signal} = 14 kHz + 15 kHz, input level sum − 3 dBr, measuring 1 kHz intermodulation)[2)]	7 to 13		0.01		%
XTALK1	Crosstalk attenuation within active audio channel pair (input level = − 3 dBr, f_{signal} = 1kHz, measuring with bandpass at 1 kHz)[2)]	8 to 13	70			dB
XTALK2	Crosstalk attenuation from a non-selected audio input pair (input level = − 3 dBr, f_{signal} = 1kHz, measuring with bandpass at 1 kHz)[2)]	7 to 13	80			dB
XTALK3	Crosstalk attenuation between audio input/output pairs (input level = − 3 dBr, f_{signal} = 1kHz, measuring with bandpass at 1 kHz)[2)]	7 to 13, 22 to 25	100			dB

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
$CHSEP_{MPX}$	Stereo separation MPX 250 Hz to 6.3 kHz 6.3 kHz to 12.5 kHz (coupling capacitor on MPX input at least 1µF)	7	 40 30			 dB dB
SNR_{MPX} 19 kHz	Suppression of unwanted signals in MPX stereo reception: 19 kHz 38 kHz 57 kHz 114 kHz measuring with bandpass at f_{signal}		 45 45 60 60			 dB dB dB dB
SNR_{RDS2}	Alias Band Suppression in RDS Channel (f_{signal} = 57 kHz, input level = 55 mV_{PP}) @ 171 kHz @ 285 kHz	6, 7	 60 70			 dB dB
SNR_{AVC}	SNR A/D3 selected AVC channel (Noise measurement RMS unweighted, BW = 0 to 4 kHz, input level = − 20 dBr, f_{signal} = 1 kHz)	2		40		dB
SNR_{AD4}	SNR A/D4 (Noise measurement RMS unweighted, BW = 0 to 7 kHz, input level = − 20 dBr, f_{signal} = 1 kHz)	1, 67, 68		50		dB
THD_{AVC}	THD A/D3 selected AVC channel (RMS unweighted, BW = 0 to 4 kHz, input level = − 3 dBr, f_{signal} = 1 kHz)	2		2.2		%
THD_{AD4}	THD A/D4 (RMS unweighted, BW = 0 to 7 kHz, input level = − 3 dBr, f_{signal} = 1 kHz	1, 67, 68		3.2		%
BW_{ADDA}	3 dB Bandwidth A/D to D/A TAPE, AUX (not provided in production test)	10 to 13, 22 to 25	18			kHz
BW_{DA}	3 dB Bandwidth D/A @f_S=32 kHz @f_S=44.1 kHz (not provided in production test)	22 to 25	 15 20			 kHz kHz
dG_{AD}	Channel deviation within active input pair: AUX, TAPE AM	8 to 13			 0.5 0.7	dB
dG_{DA}	Channel deviation within each output of: RR, RF, LR, LF Analog attenuation = 0 to − 30 dB = − 31.5 to − 45 dB	22 to 25			 0.5 0.9	 dB

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
dG_{AVOL}	Analog Volume Step Size (−45 dB to 0 dB)	22 to 25	1.4	1.5	1.6	dB
I_{REIL}	$\overline{\text{Reset}}$ Input Leakage Current	40	−10	–	+10	µA
I_{SUP}	Supply Current VSUPD VSUPA VSUP1 VSUP2	61 21 31 30	60 12 8 1.4	85 20 11 2.2	110 28 14 3	mA
V_{IMOL}	IM Bus Data Output Low Voltage	41	–	–	0.4	V
V_{IMOH}	IM Bus Data Output High Voltage		2.8	–	–	V
I_{IMOHL}	IM Bus Data Output High-Impedance Leakage Current		−10	–	+10	µA
I_{IMIL}	IM Bus Input Leakage Current		−10	–	+10	µA
V_{TOH} V_{TOL}	Digital Output High Voltage Digital Output Low Voltage	57 to 59	4.0	–	 0.4	V
V_{TIH} V_{TIL}	Digital Input High Voltage Digital Input Low Voltage	46 to 48	2.4	–	 0.8	V
V_{TUNOUT}	Synthesizer Output Voltage AMTUNOUT, FMTUNOUT	27, 29	1.1	–	V_{SUP2} −1.1	V
V_{AGNDC0}	AGNDC Open Circuit Voltage	18	2.15	2.25	2.35	V
$R_{OUTAGND}$	AGNDC Output Resistance at 27 °C at −20 to +85 °C	 18	 110 70	 125	 140 230	 kΩ kΩ
dV_{BAGNDC}	Dev. of BAGNDC from AGNDC Vol.	17, 18	−20		+20	mV
$R_{OUTBAGND}$	BAGNDC Output Resistance (f_{signal} = 1kHz, i = 0.1 mA)	17		6		Ω
dV_{DAC}	Deviation of DC Level at Audio Outputs from AGNDC Voltage	18, 22 to 25	−20		+20	mV
$I_{OUTSYNTH}$	Synthesizer Current Source Accuracy	27, 29	3.3 33 330	5 50 500	6.5 70 740	µA
PSRR	Power Supply Rejection Ratio 1 kHz 20 Hz to 20 kHz	21, 61, 31, 30, 22 to 25	 50	 40		dB
dV_{TUNOUT}	Residual Noise of Synthes. Output Volt. (BW 22Hz to 22 kHz, i = 5 µA)			2.2		µV

[1] CD-Mode, f_S = 44.1 kHz
[2] unused analog inputs connected to ground

4. Starting the Processor

After power-up, the crystal oscillator has to have been started before the Reset reaches high level. An additional wait time of 0.4 ms has to be taken into account because of a DSP-internal self-test algorithm. Then a defined start of the system can take place. Fig. 4–1 shows the complete startup sequence of the typical application.

The DCO register is loaded with a precisely defined-mean value.

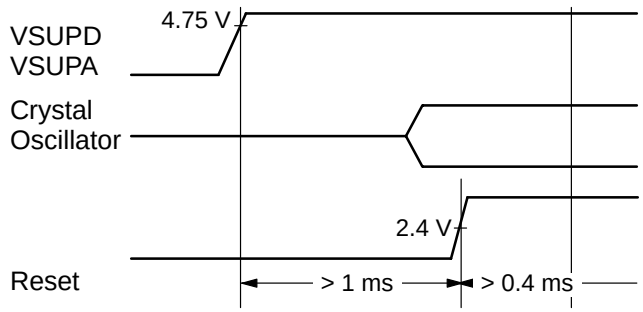


Fig. 4–1: Startup sequence

5. Synthesizer

With the synthesizer block in the CAP 3001 A, a PLL tuning system can be implemented for FM and AM receivers. The signal picked up from the mixing oscillators of the FM and AM tuners can be fed to the synthesizer block by means of highly sensitive input pins. Freely programmable dividers, operating with frequencies up to and over 100 MHz, scale the incoming signals to a reference frequency of 25 kHz. This holds true even in the case of AM, which gives AM tuning a considerable speed improvement over common designs. In order to get a tuning step size of down to 300 Hz, the reference divider is also programmable. Incoming frequencies in the range of 0.5 MHz up to more than 100 MHz can be handled, so that the designer is free to choose either a 10.7 MHz or a 450 to 460 kHz IF frequency for the AM case. The common reference frequency for AM and FM allows the implementation of a common PLL filter for the tuning output.

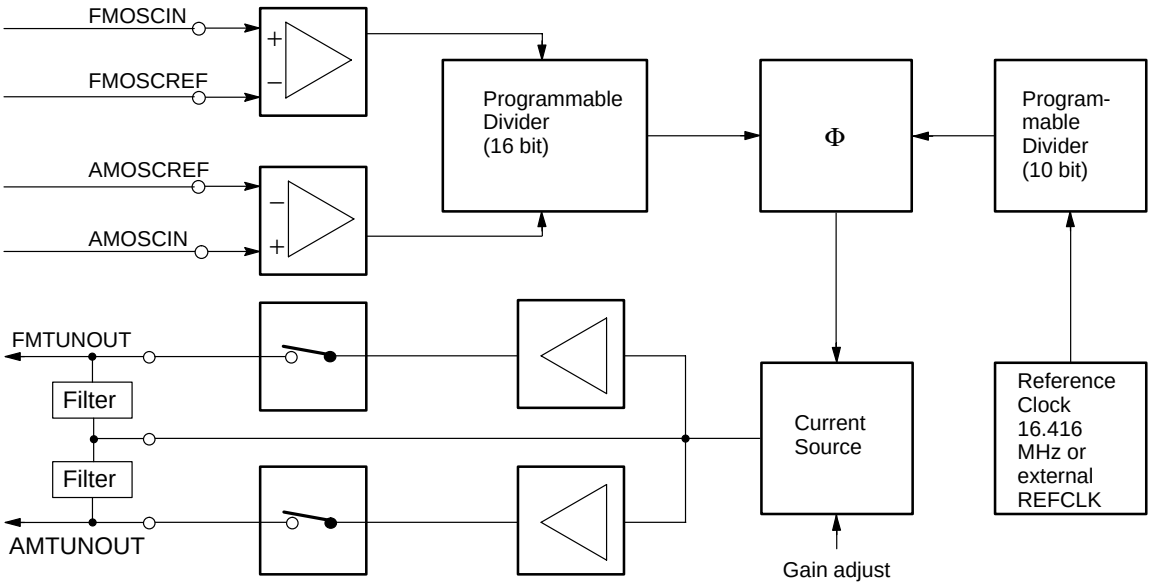


Fig. 5–1: Synthesizer block diagram

6. Application Notes

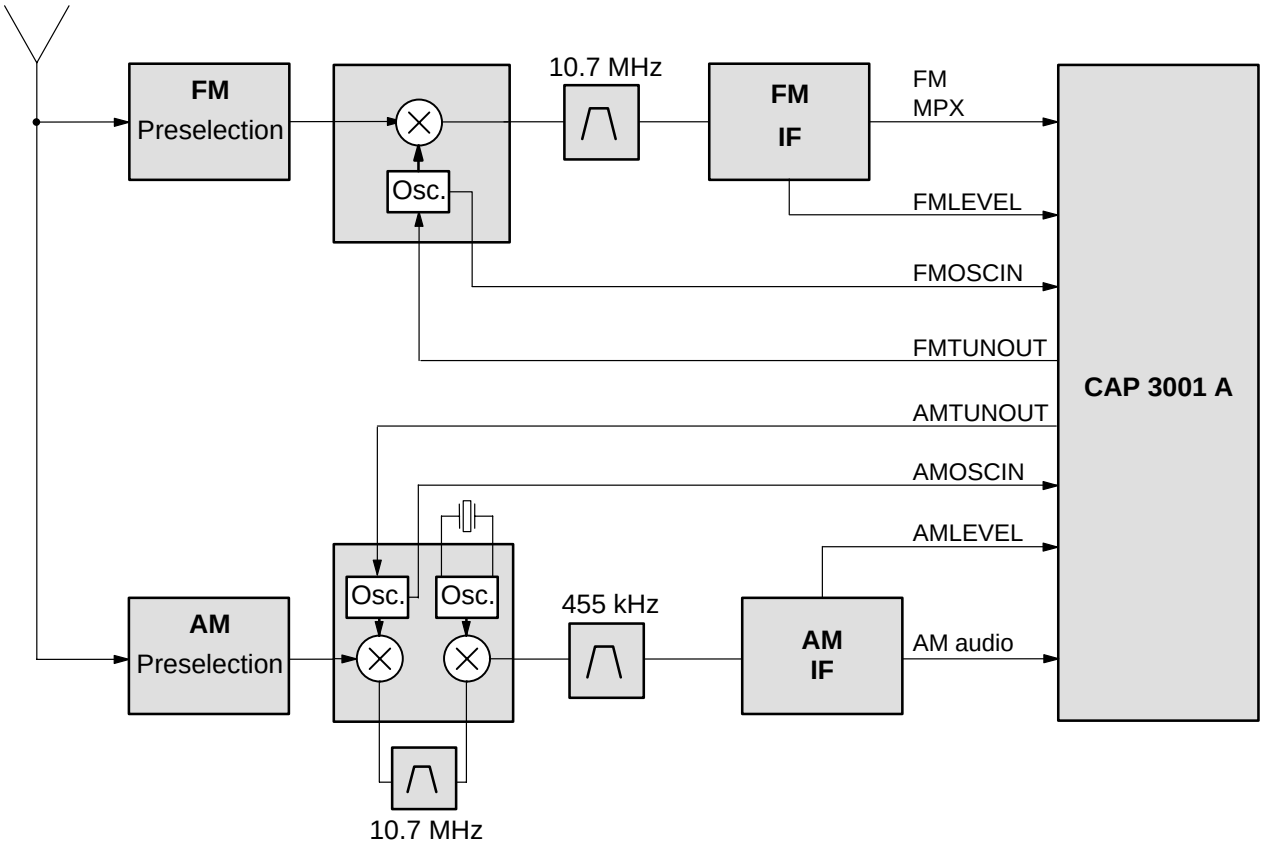
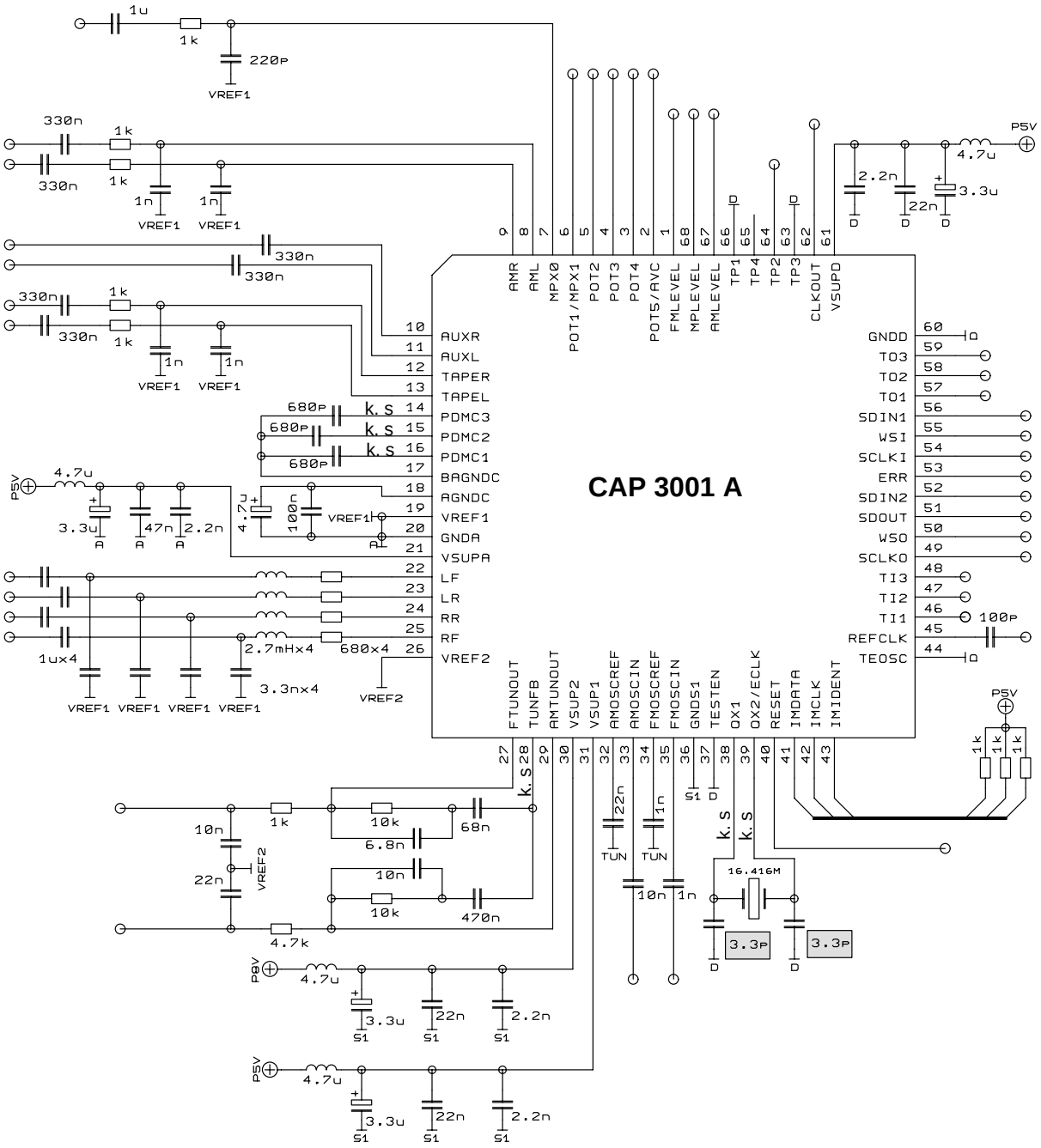


Fig. 6–1: CAP 3001 A application for 10.7 MHz AM-IF in detail

7. Typical Application Circuit



3.3P	These values have to be adjusted to achieve the neccessary pulling range (compensation of the parasitic boardcapacities).
A D S1 VREF1 TUN	These ground nets are connected together to the main ground under the IC, close to the pin VREF1.
VREF2	Pin VREF2 is the reference for the tuning synthesizer. It is connected to the tuner ground and has no direct connection to the main ground under the IC.
TUN	This is the ground at the tuner. It has a separate connection to the main ground under the IC.
k. s.	Keep these leads as short as possible!

8. Index

9. Data Sheet History:

1. Final data sheet: “CAP 3001 A Car Audio Processor Hardware”, April 4, 1996, 6251-365-1DS. First release of the final data sheet.

MICRONAS INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@intermetall.de
Internet: http://www.intermetall.de

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