CAT130044

Voltage Supervisor with Watchdog Timer and Microwire Serial EEPROM

ON Semiconductor®

http://onsemi.com

SOIC−8
W SUFFIX
CASE 751BD

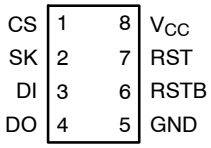
Description

CAT130044 is a voltage supervisor with a watchdog timer and serial EEPROM. This device generates a 140 ms reset pulse whenever the supply voltage falls below a preset threshold, or when there is no activity on the CS pin for 1.6 seconds. It also contains 4 kbits of EEPROM that can be written and read using the standard Microwire serial protocol.

Features

- Accurate Under Voltage System Monitoring
- High Speed Operation: 2 MHz
- 1.8 V to 5.5 V Supply Voltage Range
- Reset Output Valid with Vcc > 1 V
- Sequential Read
- Software Write Protection
- Power−up Inadvertent Write Protection
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Operating Range from −40°C to +85°C
- 8−lead Package
- These Devices are Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

PIN CONFIGURATION



SOIC (W)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

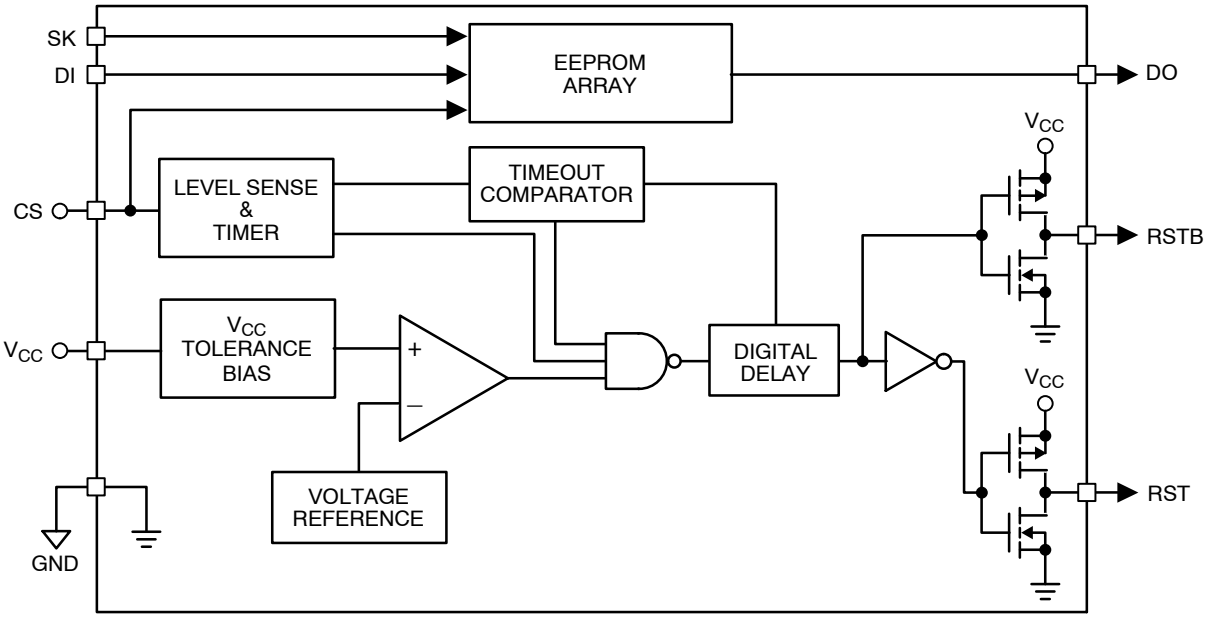


Figure 1. Block Diagram

© Semiconductor Components Industries, LLC, 2012

Table 1. PIN FUNCTION

Pin Name	Function	Pin Name	Function
CS	Chip Select and Watchdog Monitor Input	V_{CC}	Power Supply
SK	Clock Input	GND	Ground
DI	Serial Data Input	RST	Reset output (high)
DO	Serial Data Output	RSTB	Reset output (low)

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.3 to +6.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (DC Characteristics: V_{CC} = 2.0 V to 3.6 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted. Typical Values at T_A = 25°C and V_{CC} = 3.0 V.) (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{RST}	Reset Threshold	CAT130044, R option	2.55	2.63	2.70	V
	Reset Threshold Tempco			40		ppm/°C
	Reset Threshold Hysteresis			5		mV
t_{RD}	V_{CC} to Reset Delay (Note 3)	V_{CC} = V_{TH} to (V_{TH} − 100 mV)		20		μs
t_{RP}	Reset Active Timeout Period		140	200	400	ms
V_{OH}	RSTB Output High Voltage	V_{CC} = $V_{RST\ max}$, I_{SOURCE} = −30 μA	0.8 x V_{CC}			V
V_{OL}	RSTB Output Low Voltage	V_{CC} = $V_{RST\ min}$, I_{SINK} = 1.2 mA			0.3	V
		T_A = 0°C to +70°C, V_{CC} = 1 V, V_{CC} falling, I_{SINK} = 50 μA			0.3	
		T_A = T_{MIN} to T_{MAX}, V_{CC} = 1.2 V, V_{CC} falling, I_{SINK} = 100 μA			0.3	
I_{SOURCE}	RSTB Output Short−Circuit Current	Reset = 0 V, V_{CC} = 5.5 V			1.5	mA
		Reset = 0 V, V_{CC} = 3.6 V			0.8	
V_{OH}	RST Output Voltage	V_{CC} > 1.8 V, I_{SOURCE} = −150 μA	0.8 x V_{CC}			V
V_{OL}		V_{CC} = $V_{RST\ max}$, I_{SINK} = 1.2 mA			0.3	
WATCHDOG INPUT						
t_{WD}	Watchdog Timeout Period		1.12	1.60	3.20	s
t_{WDI}	CS Pulse Width	V_{IL} = 0.4 V, V_{IH} = 0.8 x V_{CC}	50			ns
	CS Input Current (Note 4)	CS = V_{CC}, Time Average		120	160	μA
		CS = 0 V, Time Average	−20	−15		

2. Over−temperature limits are guaranteed by design and not production tested.
3. The RESET short−circuit current is the maximum pull−up current when reset is driven low by a bidirectional output.
4. The CS input current is specified as an average input current when the CS input is driven high or low. To clock the CS input in the active mode the drive device must be able to source or sink at least 200 μA when active.

Table 4. SERIAL EEPROM RELIABILITY CHARACTERISTICS (Note 5)

Symbol	Parameter	Min	Units
N_{END} (Note 6)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
6. Block Mode, V_{CC} = 5 V, 25°C.

Table 5. SERIAL EEPROM D.C. OPERATING CHARACTERISTICS
(V_{CC} = +1.8 V to +5.5 V, T_A = −40°C to +85°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1 MHz, V_{CC} = 5.0 V		1	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1 MHz, V_{CC} = 5.0 V		500	μA
I_{SB1}	Power Supply Current (Standby)	V_{IN} = GND or V_{CC}, CS = GND		20	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, CS = GND		1	μA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V	−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 4.5 V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 4.5 V	V_{CC} x 0.7	V_{CC} + 1	V
$V_{OL1:DO}$	DO Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 2.1 mA		0.4	V
$V_{OH1:DO}$	DO Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = −400 μA	2.4		V
$V_{OL2:DO}$	DO Output Low Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA		0.2	V
$V_{OH2:DO}$	DO Output High Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OH} = −100 μA	V_{CC} − 0.2		V

Table 6. PIN CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT} (Note 7)	Output Capacitance (DO)	V_{OUT} = 0 V			5	pF
C_{IN} (Note 7)	Input Capacitance (SK, DI)	V_{IN} = 0 V			5	pF

7. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 7. SERIAL EEPROM A.C. CHARACTERISTICS
(V_{CC} = +1.8 V to +5.5 V, T_A = −40°C to +85°C, unless otherwise specified.) (Note 8)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	μs
t_{PD0}	Output Delay to 0		0.25	μs
t_{HZ} (Note 9)	Output Delay to High−Z		100	ns
t_{EW}	Program/Erase Pulse Width		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		μs
t_{SKHI}	Minimum SK High Time	0.25		μs
t_{SKLOW}	Minimum SK Low Time	0.25		μs
t_{SV}	Output Delay to Status Valid		0.25	μs
SK_{MAX}	Maximum Clock Frequency	DC	2000	kHz

8. Test conditions according to “A.C. Test Conditions” table.
9. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 8. SERIAL EEPROM POWER−UP TIMING (Notes 10, 11)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

10. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
11. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 9. SERIAL EEPROM A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	0.2 V_{CC} to 0.7 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	0.5 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Output Load	Current Source I_{OLmax}/I_{OHmax}; CL = 100 pF	

Device Operation

Processor RESET

The CAT130044 detects supply voltage (V_{CC}) conditions that are below the specified voltage trip value (V_{RST}) and provide a reset output to maintain correct system operation. On power−up, RST and RSTB are kept active for a minimum delay tRP of 140 ms after the supply voltage (V_{CC}) rises above V_{RST} to allow the power supply and processor to stabilize. When V_{CC} drops below the voltage trip value (V_{RST}), the reset output signals RST and RSTB are pulled active. RST and RSTB specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

Watchdog Timer

The CAT130044 uses the Chip Select input as a Watchdog input. The watchdog timer function forces the RST and RSTB signals active when the CS input does not have a transition from low−to−high or high−to−low within 1.12 seconds. Timeout of the watchdog starts when RST and RSTB become inactive. If a transition occurs on the CS input pin prior to the watchdog time−out, the watchdog timer is reset and begins to time−out again. If the watchdog timer is allowed to time−out, then the reset outputs will go active for t_{RP} and once released will repeat the watchdog timeout process.

Figure below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be used to strobe the watchdog input.

For the most efficient operation the CS input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

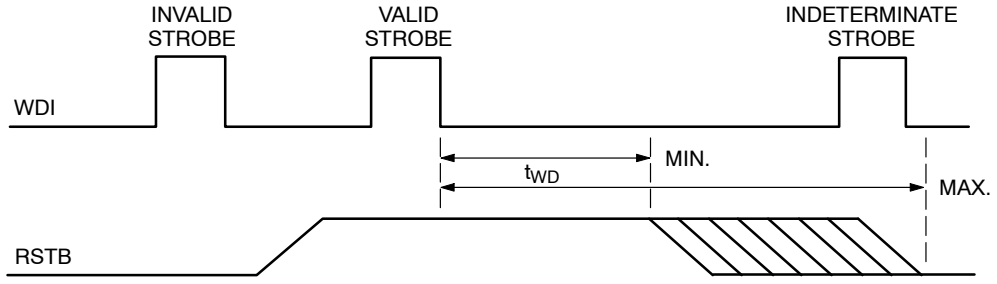


Figure 2. Timing Diagram – Strobe Input

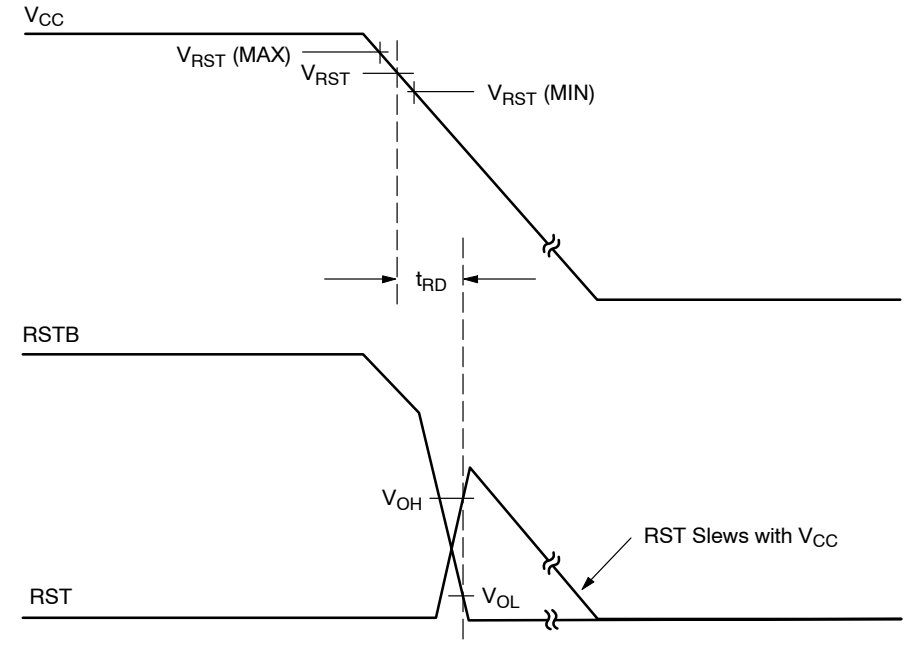


Figure 3. Timing Diagram – Power Down

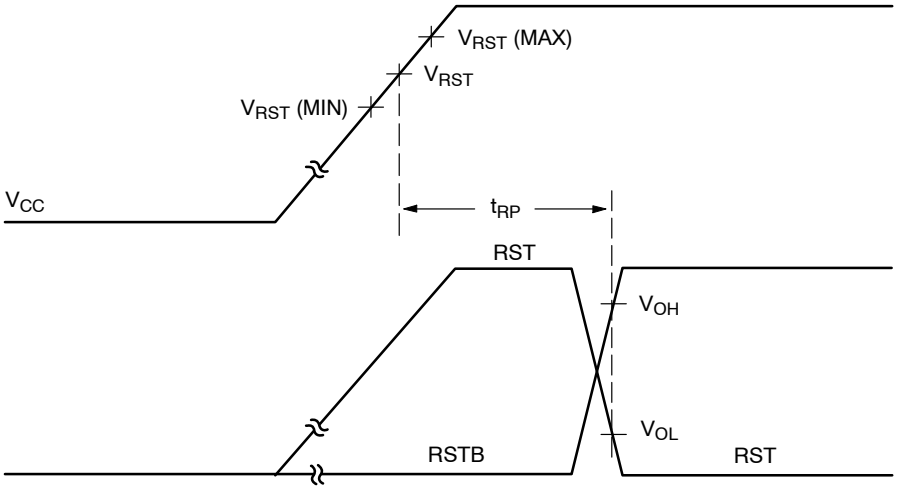


Figure 4. Timing Diagram – Power Up

CAT130044 contains a 4096−bit nonvolatile memory intended for use with industry standard microprocessors. It is organized in 8 bit words. The device operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 5.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2−bit (or 4−bit) opcode, 9−bit address and for write operations an 8−bit data field. The instruction format is shown in Instruction Set table.

Table 10. INSTRUCTION SET

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	A8−A0		Read Address AN − A0
ERASE	1	11	A8−A0		Clear Address AN − A0
WRITE	1	01	A8−A0	D7−D0	Write Address AN − A0
EWEN	1	00	11XXXXXXX		Write Enable
EWDS	1	00	00XXXXXXX		Write Disable
ERAL	1	00	10XXXXXXX		Clear All Addresses
WRAL	1	00	01XXXXXXX	D7−D0	Write All Addresses

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT130044 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAT130044 after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 6.

Erase/Write Enable and Disable

The device powers up in the write disable state. Any writing after power−up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT130044 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 7.

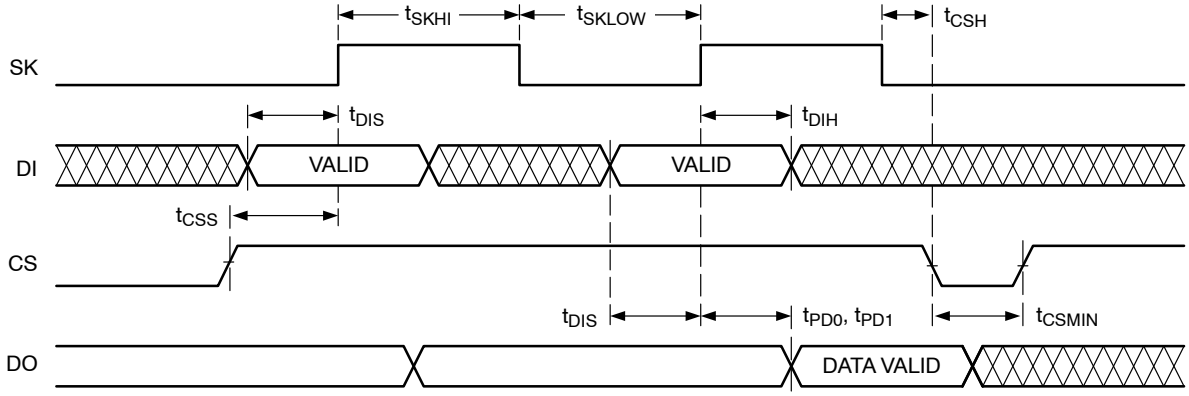


Figure 5. Synchronous Data Timing

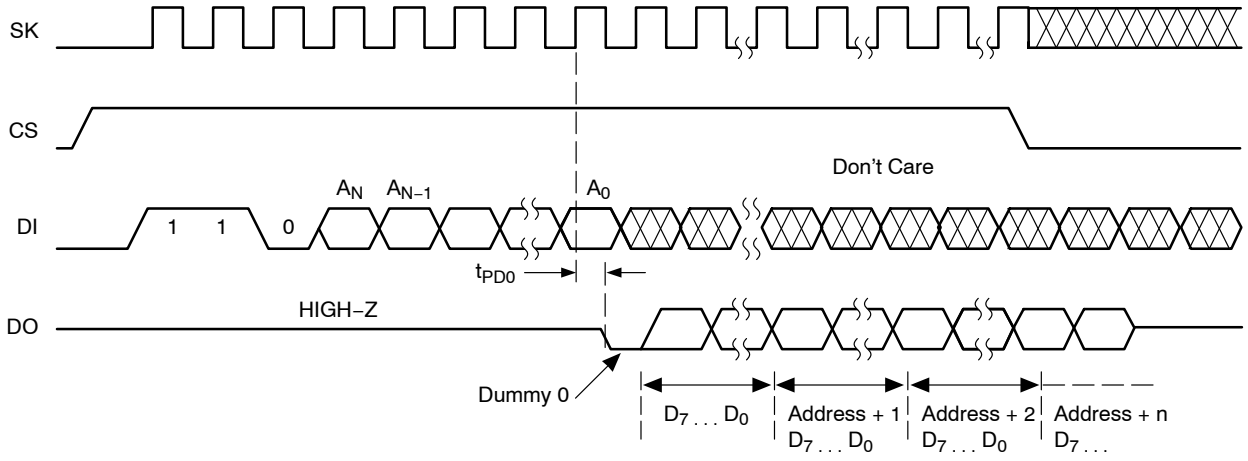


Figure 6. READ Instruction Timing

Write

After receiving a WRITE command (Figure 8), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130044 can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 9). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130044 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

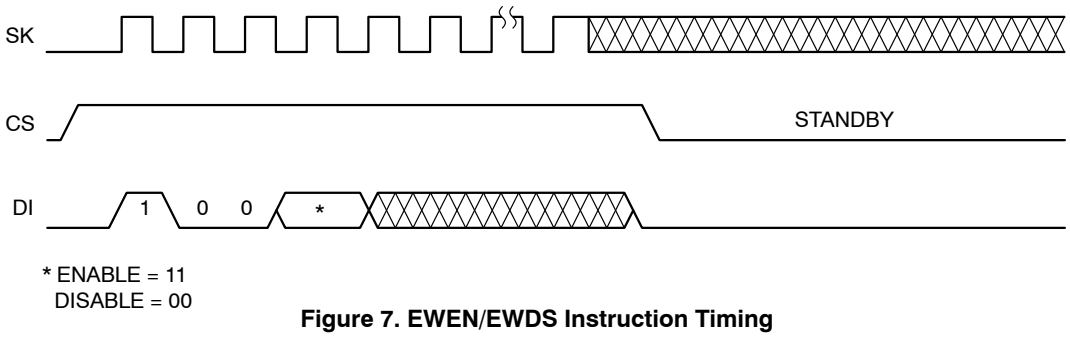


Figure 7. EWEN/EWDS Instruction Timing

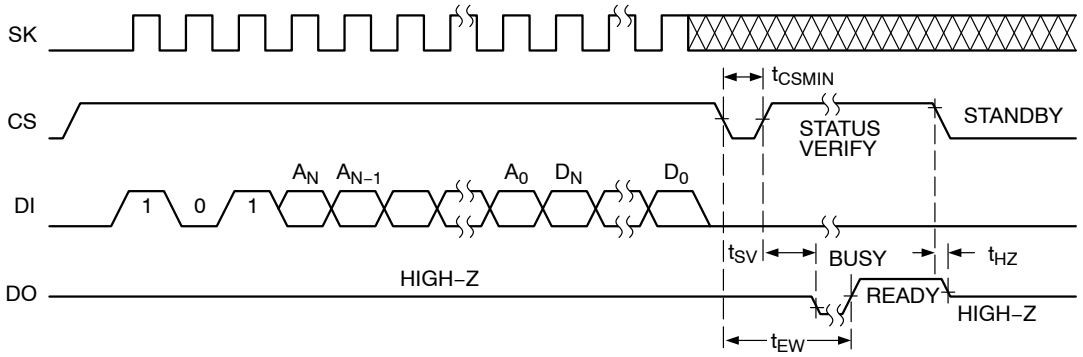


Figure 8. Write Instruction Timing

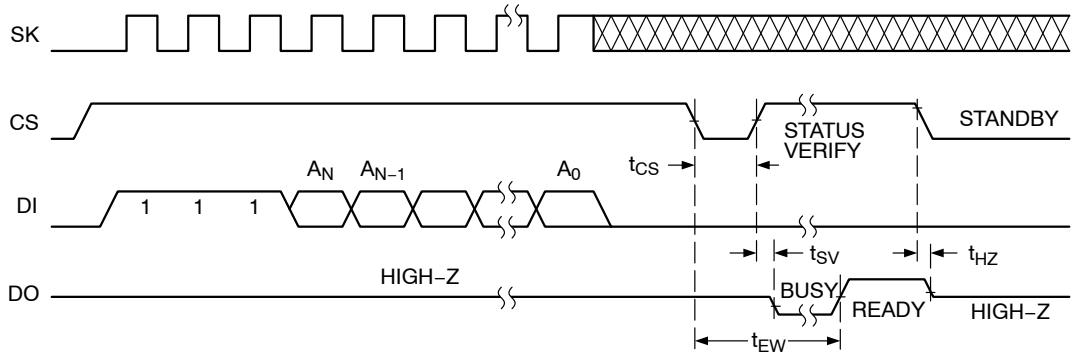


Figure 9. Erase Instruction Timing

Erase All

Upon receiving an ERAL command (Figure 10), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 11). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

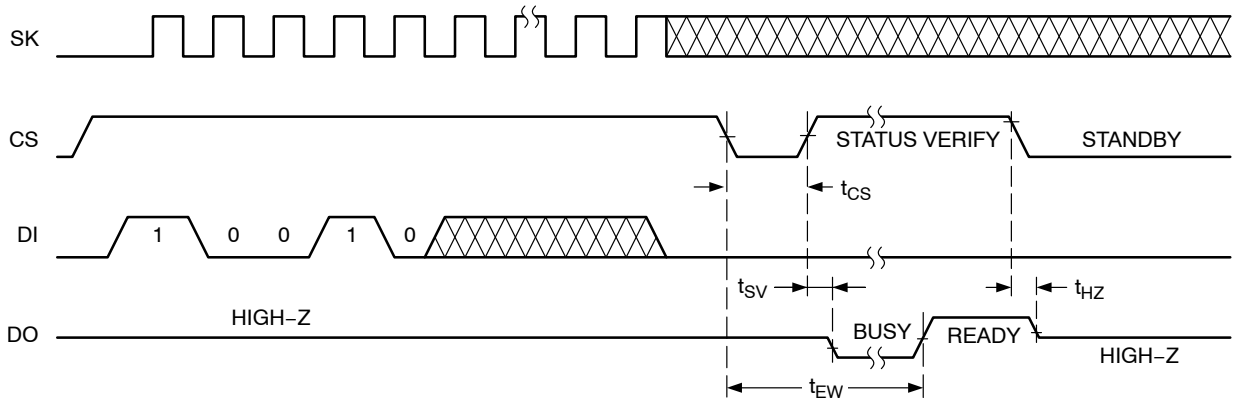


Figure 10. ERAL Instruction Timing

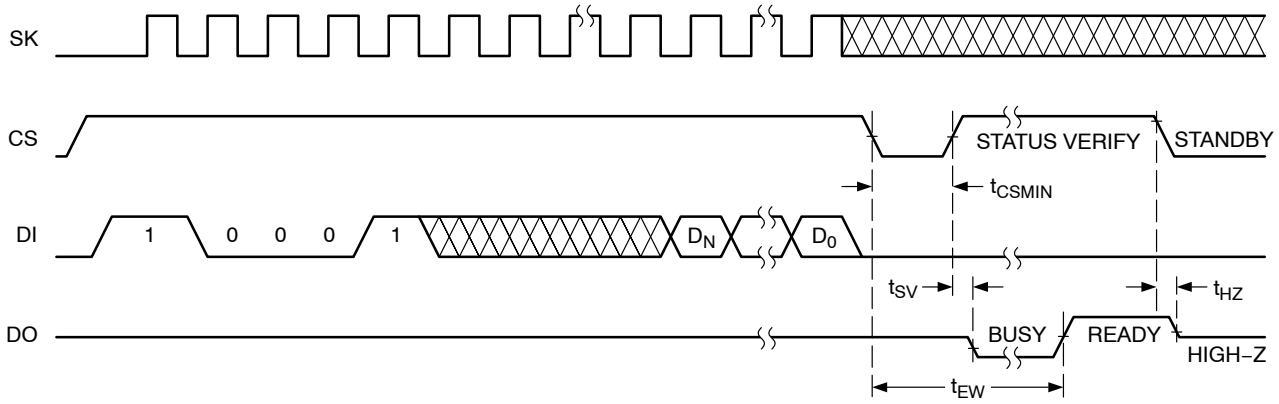


Figure 11. WRAL Instruction Timing

Application Notes

μP’s with Bidirectional Reset Pins

The RSTB output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT130044 is 800 μA), allowing the processor to pull the output low even when the CAT130044 is pulling it high.

Power Transients

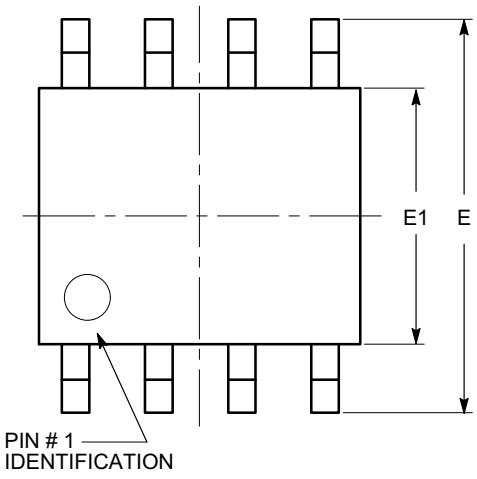
Generally short duration negative−going transients of less than 2 μs on the power supply at V_{RST} minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

Output Valid Conditions

The RSTB output uses a push−pull output which can maintain a valid output down to a V_{CC} of 1.0 volts. To sink current below 0.8 V a resistor can be connected from RSTB to Ground. This arrangement will maintain a valid value on the RSTB output during both power up and down but will draw current when the RSTB output is in the high state. A resistor value of about 100 kΩ should be adequate in most situations to maintain a low condition valid output down to V_{CC} equal to 0 V.

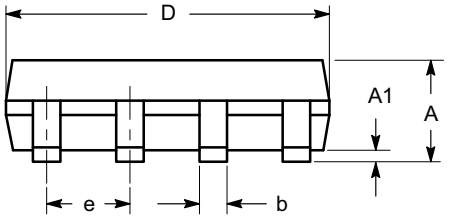
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

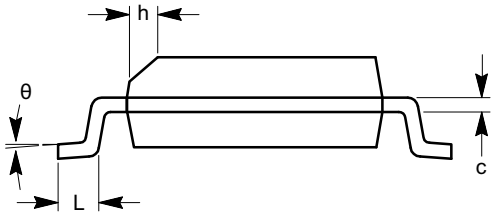


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 11. ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping
CAT130044RWI−GT3	1344GA	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

12. All packages are RoHS−compliant (Lead−free, Halogen−free).
13. The standard lead finish is NiPdAu.
14. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
15. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
16. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative