



CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

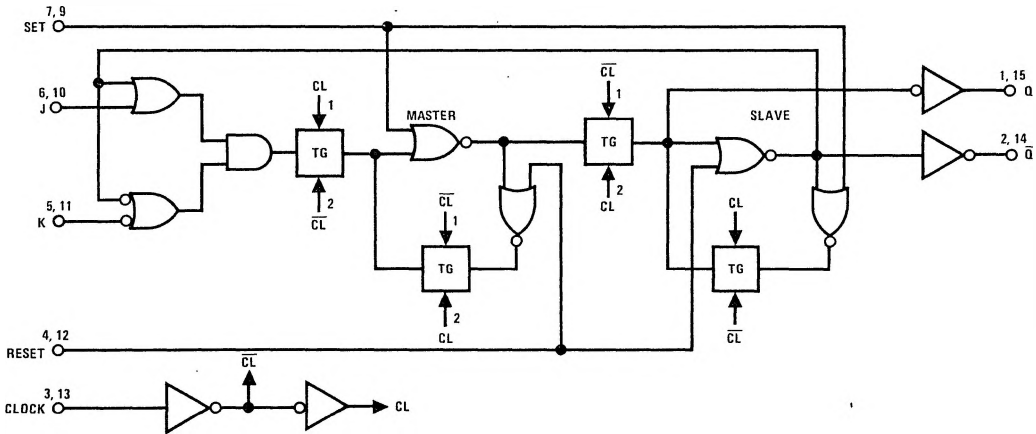
These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and "Q̄" outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

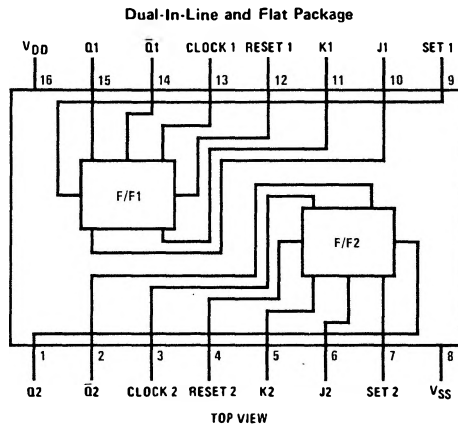
Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Low power 50 nW (typ.)
- Medium speed operation 12 MHz (typ.) with 10V supply

Schematic Diagram



Connection Diagram



Absolute Maximum Ratings (Notes 1 and 2)

V _{DD} dc Supply Voltage	-0.5 to +18 V _{DC}
V _{IN} Input Voltage	-0.5 to V _{DD} + 0.5 V _{DC}
T _S Storage Temperature Range	-65°C to +150°C
P _D Package Dissipation	500 mW
T _L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)	
V _{DD} dc Supply Voltage	3 to 15 V _{DC}
V _{IN} Input Voltage	0 to V _{DD} V _{DC}
T _A Operating Temperature Range	-55°C to +125°C
CD4027BM	-40°C to +85°C
CD4027BC	

DC Electrical Characteristics CD4027BM (Note 2)

PARAMETER	CONDITIONS	55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I _{DD} Quiescent Device Current	V _{DD} = 5V		1			1		30	μA
	V _{DD} = 10V		2			2		60	μA
	V _{DD} = 15V		4			4		120	μA
V _{OL} Low Level Output Voltage	I _O < 1μA								
	V _{DD} = 5V		0.05		0	0.05		0.05	V
	V _{DD} = 10V		0.05		0	0.05		0.05	V
V _{OH} High Level Output Voltage	I _O < 1μA								
	V _{DD} = 5V	4.95		4.95	5		4.95		V
	V _{DD} = 10V	9.95		9.95	10		9.95		V
V _{IL} Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
	V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.64		0.51	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.6		1.3	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	4.2		3.4	8.8		2.4		mA
I _{OH} High Level Output Current	V _{DD} = 5V, V _O = 4.6V	-0.64		-0.51	-0.88		-0.36		mA
	V _{DD} = 10V, V _O = 9.5V	-1.6		-1.3	-2.25		-0.9		mA
	V _{DD} = 15V, V _O = 13.5V	-4.2		-3.4	-8.8		-2.4		mA
I _{IN} Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.1		-10 ⁻⁵	-0.1		-1.0	μA
	V _{DD} = 15V, V _{IN} = 15V		0.1		10 ⁻⁵	0.1		1.0	μA

DC Electrical Characteristics (Cont'd.) CD4027BC (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I _{DD} Quiescent Device Current	V _{DD} = 5V		4			4		30	μA
	V _{DD} = 10V		8			8		60	μA
	V _{DD} = 15V		16			16		120	μA
V _{OL} Low Level Output Voltage	I _O < 1μA								
	V _{DD} = 5V		0.05		0	0.05		0.05	V
	V _{DD} = 10V		0.05		0	0.05		0.05	V
V _{OH} High Level Output Voltage	I _O < 1μA								
	V _{DD} = 5V	4.95		4.95	5		4.95		V
	V _{DD} = 10V	9.95		9.95	10		9.95		V
V _{IL} Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
	V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics CD4027BC (Note 2)

PARAMETER	CONDITIONS	-40 C		25 C			85 C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10^{-5}	-0.3		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25^\circ C, C_L = 50 pF, t_{rCL} = t_{fCL} = 20 ns$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH} Propagation Delay Time From Clock to Q or \bar{Q}	$V_{DD} = 5V$		200	400	ns
	$V_{DD} = 10V$		80	160	ns
	$V_{DD} = 15V$		65	130	ns
t_{PHL} or t_{PLH} Propagation Delay Time From Set to \bar{Q} or Reset to Q	$V_{DD} = 5V$		170	340	ns
	$V_{DD} = 10V$		70	140	ns
	$V_{DD} = 15V$		55	110	ns
t_{PHL} or t_{PLH} Propagation Delay Time From Set to Q or Reset to \bar{Q}	$V_{DD} = 5V$		110	220	ns
	$V_{DD} = 10V$		50	100	ns
	$V_{DD} = 15V$		40	80	ns
t_s Minimum Data Set-Up Time	$V_{DD} = 5V$		135	270	ns
	$V_{DD} = 10V$		55	110	ns
	$V_{DD} = 15V$		45	90	ns
t_{THL} or t_{TLH} Transition Time	$V_{DD} = 5V$		100	200	ns
	$V_{DD} = 10V$		50	100	ns
	$V_{DD} = 15V$		40	80	ns
f_{CL} Maximum Clock Frequency (Toggle Mode)	$V_{DD} = 5V$	2.5	5		MHz
	$V_{DD} = 10V$	6.2	12.5		MHz
	$V_{DD} = 15V$	7.6	15.5		MHz
t_{rCL} or t_{fCL} Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
	$V_{DD} = 10V$	10			μs
	$V_{DD} = 15V$	5			μs
t_W Minimum Clock Pulse Width ($t_{WH} = t_{WL}$)	$V_{DD} = 5V$		100	200	ns
	$V_{DD} = 10V$		40	80	ns
	$V_{DD} = 15V$		32	65	ns
t_{WH} Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		80	160	ns
	$V_{DD} = 10V$		30	60	ns
	$V_{DD} = 15V$		25	50	ns
C_{IN} Average Input Capacitance	Any Input		5	7.5	pF
C_{PD} Power Dissipation Capacity	Per Flip-Flop (Note 3)		35		pF

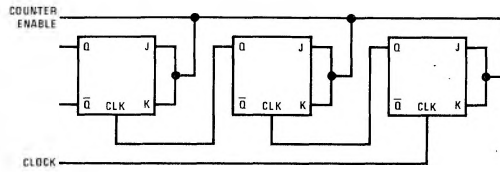
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

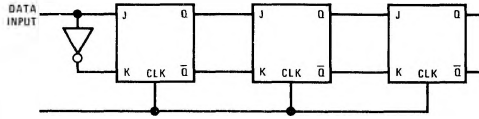
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

Typical Applications

Ripple Binary Counters



Shift Registers



Truth Table

* _{t_{n-1}} INPUTS						* _{t_n} OUTPUTS	
CL [▲]	J	K	S	R	Q	Q	\bar{Q}
	1	X	0	0	0	1	0
	X	0	0	0	1	1	0
	0	X	0	0	0	0	1
	X	1	0	0	1	0	1
	X	X	0	0	X	(No change)	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

- Where:
- 1 = High Level
 - 0 = Low Level
 - ▲ = Level Change
 - X = Don't Care
 - = t_{n-1} refers to the time interval prior to the positive clock pulse transition
 - ♦ = t_n refers to the time intervals after the positive clock pulse transition