



# CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate

# CD4075BM/CD4075BC Double Buffered Triple 3-Input OR Gate

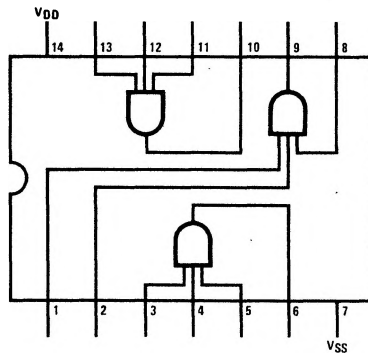
## General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

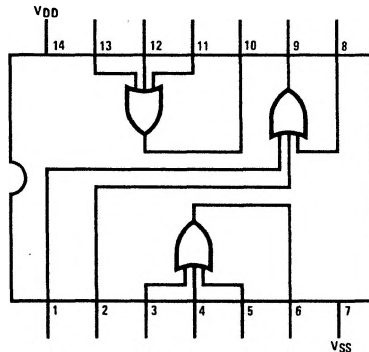
## Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45  $V_{DD}$  typ.
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V - 10V - 15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage  $1\mu A$  at 15V over full temperature range

## Connection Diagrams



CD4073 Triple 3-Input AND Gate  
TOP VIEW



CD4075B Triple 3-Input OR Gate  
TOP VIEW

### Absolute Maximum Ratings (Notes 1 and 2)

$V_{DD}$	DC Supply Voltage	-0.5 $V_{DC}$ to +18 $V_{DC}$
$V_{IN}$	Input Voltage	-0.5 $V_{DC}$ to $V_{DD} + 0.5 V_{DC}$
$T_S$	Storage Temperature Range	-65°C to +150°C
$P_D$	Package Dissipation	500 mW
$T_L$	Lead Temperature (soldering, 10 seconds)	300°C

### Operating Conditions (Note 2)

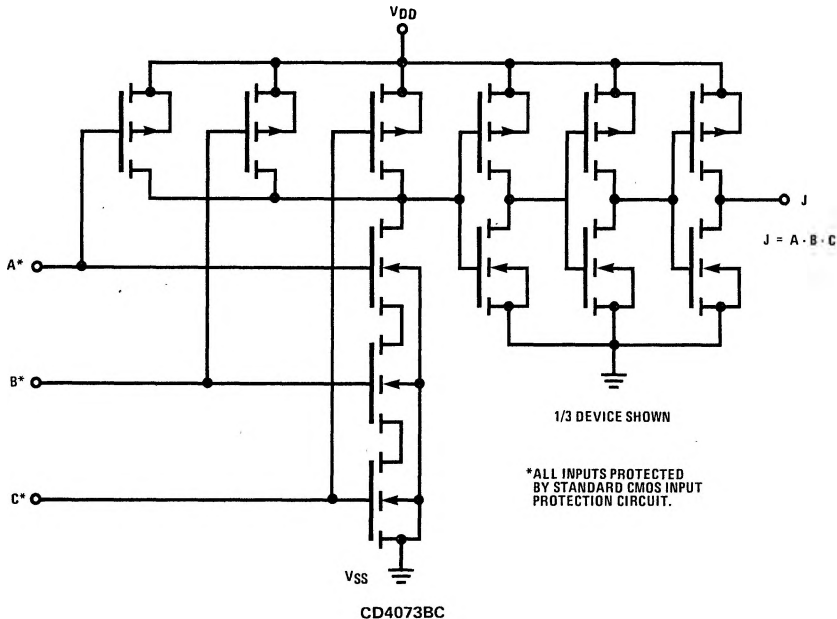
$V_{DD}$	DC Supply Voltage	+5 $V_{DC}$ to +15 $V_{DC}$
$V_{IN}$	Input Voltage	0 $V_{DC}$ to $V_{DD} V_{DC}$
$T_A$	Operating Temperature Range	-55°C to +125°C
		CD4073BM/CD4075BM
		-40°C to +85°C
		CD4073BC/CD4075BC

### DC Electrical Characteristics CD4073BM/CD4075BM (Note 2)

PARAMETER	CONDITIONS	-55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
$I_{DD}$ Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	$\mu A$
	$V_{DD} = 10V$		0.5		0.005	0.5		15	$\mu A$
	$V_{DD} = 15V$		1.0		0.006	1.0		30	$\mu A$
$V_{OL}$ Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$	$ I_{OL}  < 1 \mu A$	0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$ High Level Output Voltage	$V_{DD} = 5V$		4.95		4.95	5		4.95	V
	$V_{DD} = 10V$	9.95		9.95	10		9.95	V	
	$V_{DD} = 15V$	14.95		14.95	15		14.95	V	
$V_{IL}$ Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
	$V_{DD} = 10V, V_O = 1.0V$	$ I_{OL}  < 1 \mu A$	3.0		4	3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
$V_{IH}$ High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$		3.5		3.5	3		3.5	V
	$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0	V	
	$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0	V	
$I_{OL}$ Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36	mA	
	$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.2		0.90	mA	
	$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8		2.4	mA	
$I_{OH}$ High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36	mA	
	$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.2		-0.90	mA	
	$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8		-2.4	mA	
$I_{IN}$ Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.10		$-10^{-5}$	-0.10		$\mu A$	
	$V_{DD} = 15V, V_{IN} = 15V$		0.10		$10^{-5}$	0.10		$\mu A$	

Notes on following page.

### Schematic Diagram



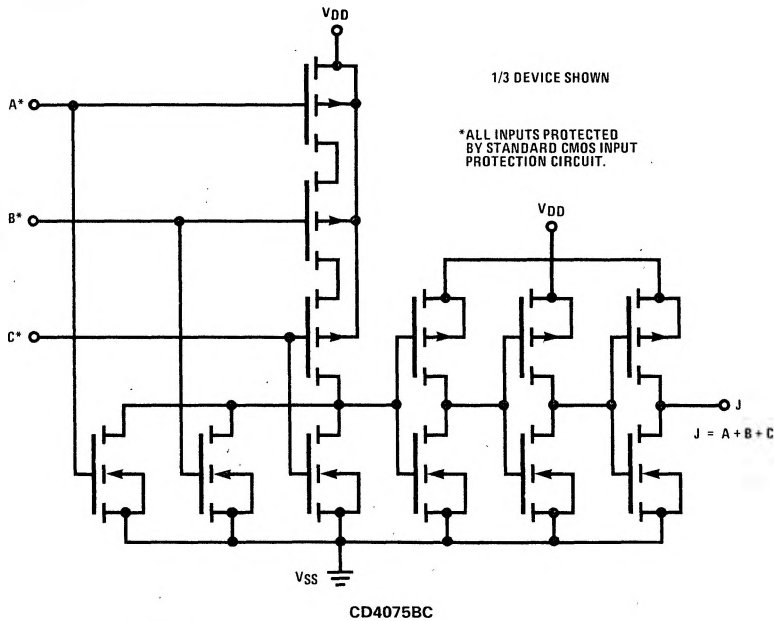
**DC Electrical Characteristics** CD4073BC/CD4075BC (Note 2)

PARAMETER	CONDITIONS	-40°C		+25°C			+85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I <sub>DD</sub>	Quiescent Device Current V <sub>DD</sub> = 5 V V <sub>DD</sub> = 10 V V <sub>DD</sub> = 15 V		1		0.004	1		7.5	μA
			2		0.005	2		15	μA
			4		0.006	4		30	μA
V <sub>OL</sub>	Low Level Output Voltage V <sub>DD</sub> = 5 V } V <sub>DD</sub> = 10 V } I <sub>OL</sub> < 1 μA V <sub>DD</sub> = 15 V }		0.05		0	0.05		0.05	V
			0.05		0	0.05		0.05	V
			0.05		0	0.05		0.05	V
V <sub>OH</sub>	High Level Output Voltage V <sub>DD</sub> = 5 V } V <sub>DD</sub> = 10 V } I <sub>OL</sub> < 1 μA V <sub>DD</sub> = 15 V }	4.95		4.95	5		4.95		V
		9.95		9.95	10		9.95		V
		14.95		14.95	15		14.95		V
V <sub>IL</sub>	Low Level Input Voltage V <sub>DD</sub> = 5 V, V <sub>O</sub> = 0.5 V } V <sub>DD</sub> = 10 V, V <sub>O</sub> = 1.0 V } I <sub>OL</sub> < 1 μA V <sub>DD</sub> = 15 V, V <sub>O</sub> = 1.5 V }		1.5		2	1.5		1.5	V
			3.0		4	3.0		3.0	V
			4.0		6	4.0		4.0	V
V <sub>IH</sub>	High Level Input Voltage V <sub>DD</sub> = 5 V, V <sub>O</sub> = 4.5 V } V <sub>DD</sub> = 10 V, V <sub>O</sub> = 9.0 V } I <sub>OL</sub> < 1 μA V <sub>DD</sub> = 15 V, V <sub>O</sub> = 13.5 V }	3.5		3.5	3		3.5		V
		7.0		7.0	6		7.0		V
		11.0		11.0	9		11.0		V
I <sub>OL</sub>	Low Level Output Current V <sub>DD</sub> = 5 V, V <sub>O</sub> = 0.4 V V <sub>DD</sub> = 10 V, V <sub>O</sub> = 0.5 V V <sub>DD</sub> = 15 V, V <sub>O</sub> = 1.5 V	0.52	0.44	0.88		0.36			mA
		1.3	1.1	2.2		0.90			mA
		3.6	3.0	8		2.4			mA
I <sub>OH</sub>	High Level Output Current V <sub>DD</sub> = 5 V, V <sub>O</sub> = 4.6 V V <sub>DD</sub> = 10 V, V <sub>O</sub> = 9.5 V V <sub>DD</sub> = 15 V, V <sub>O</sub> = 13.5 V	-0.52	-0.44	-0.88		-0.36			mA
		-1.3	-1.1	-2.2		-0.90			mA
		-3.6	-3.0	-8		-2.4			mA
I <sub>IN</sub>	Input Current V <sub>DD</sub> = 15 V, V <sub>IN</sub> = 0 V V <sub>DD</sub> = 15 V, V <sub>IN</sub> = 15 V		-0.30		-10 <sup>-5</sup>	-0.30		-1.0	μA
			0.30		10 <sup>-5</sup>	0.30		1.0	μA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** V<sub>SS</sub> = 0 V unless otherwise specified.

**Schematic Diagram**



# AC Electrical Characteristics

CD4073BM/CD4073BC/CD4075BM/CD4075BC

$T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}$  unless otherwise specified.

PARAMETER	CONDITIONS	CD4073BC CD4073BM			CD4075BC CD4075BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PHL}$ Propagation Delay, High to Low Level	$V_{DD} = 5\text{ V}$		130	250		140	250	ns
	$V_{DD} = 10\text{ V}$		60	100		70	100	ns
	$V_{DN} = 15\text{ V}$		40	70		50	70	ns
$t_{PLH}$ Propagation Delay, Low to High Level	$V_{DD} = 5\text{ V}$		140	250		130	250	ns
	$V_{DD} = 10\text{ V}$		70	100		50	100	ns
	$V_{DD} = 15\text{ V}$		50	70		40	70	ns
$t_{THL}$ Transition Time	$V_{DD} = 5\text{ V}$		90	200		90	200	ns
	$V_{DD} = 10\text{ V}$		50	100		50	100	ns
	$V_{DD} = 15\text{ V}$		40	80		40	80	ns
$C_{IN}$ Average Input Capacitance (See Note 3)	Any Input		5	7.5		5	7.5	pF
$C_{PD}$ Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4:  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

CD4073BM/CD4073BC, CD4075BM/CD4075BC