

## Dual 1:2 Low Additive Jitter LVDS Buffer

Check for Samples: [CDCLVD2102](#)

### FEATURES

- Dual 1:2 Differential Buffer
- Low Additive Jitter <300 fs RMS in 10-kHz to 20-MHz
- Low Within Bank Output Skew of 15 ps (Max)
- Universal Inputs Accept LVDS, LVPECL, LVCMOS
- One Input Dedicated for Two Outputs
- Total of 4 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency up to 800 MHz
- 2.375–2.625V Device Power Supply
- LVDS Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive Coupled Inputs
- Industrial Temperature Range –40°C to 85°C
- Packaged in 3mm × 3mm 16-Pin QFN (RGT)
- ESD Protection Exceeds 3 kV HBM, 1 kV CDM

### APPLICATIONS

- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General Purpose Clocking

### DESCRIPTION

The CDCLVD2102 clock buffer distributes two clock inputs (IN0, IN1) to a total of 4 pairs of differential LVDS clock outputs (OUT0, OUT3). Each buffer block consists of one input and 2 LVDS outputs. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD2102 is specifically designed for driving 50-Ω transmission lines. If driving the inputs in single ended mode, the appropriate bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin.

Using the control pin (EN), outputs can be either disabled or enabled. If the EN pin is left open two buffers with all outputs are enabled, if switched to a logical "0" both buffers with all outputs are disabled (static logical "0"), if switched to a logical "1", one buffer with two outputs is disabled and another buffer with two outputs is enabled. The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD2102 is packaged in small 16-pin, 3-mm × 3-mm QFN package.

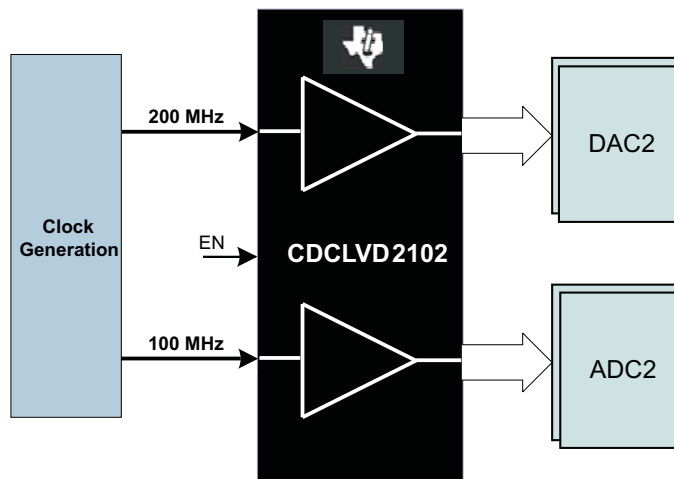


Figure 1. Application Example



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

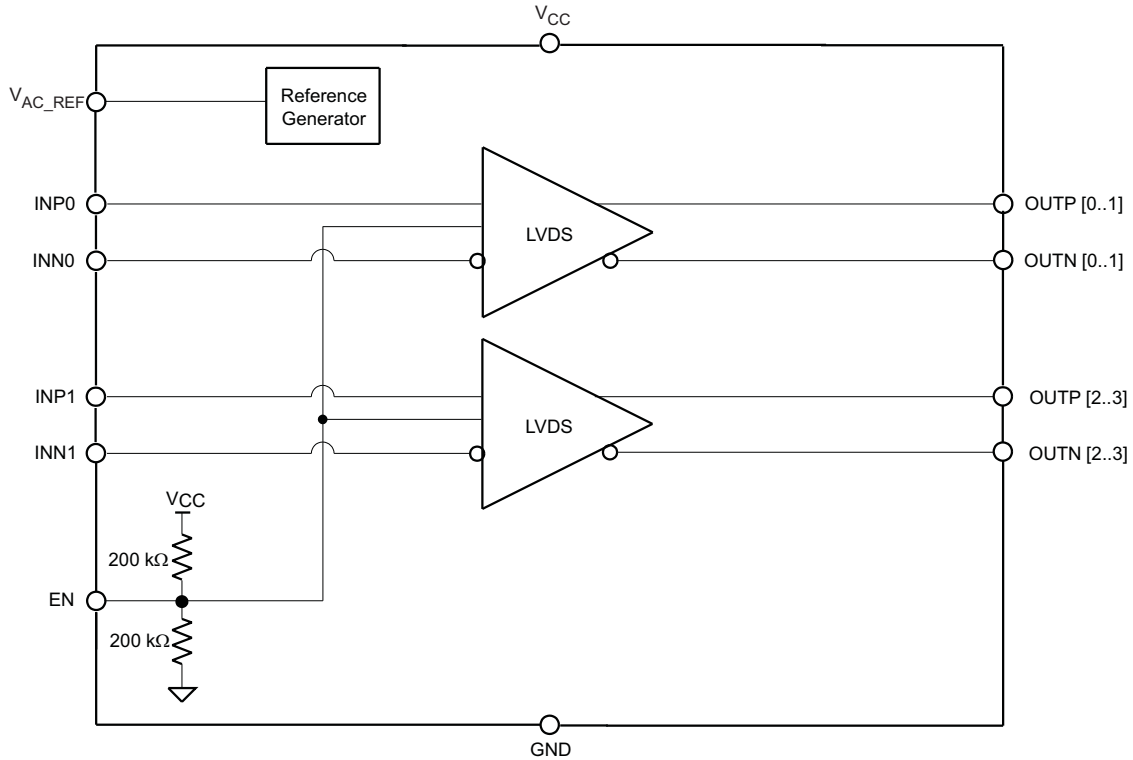
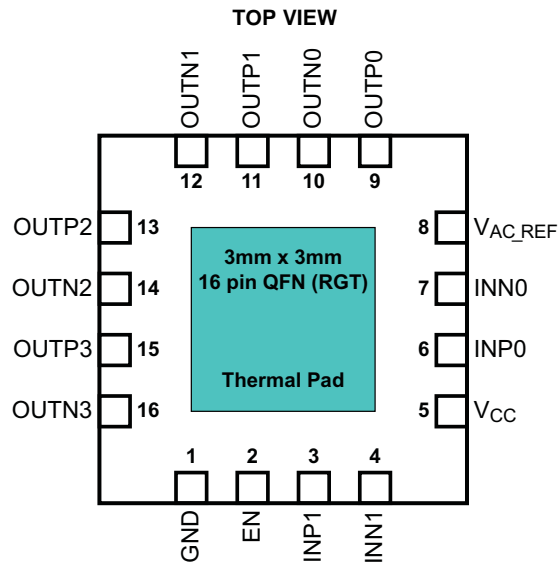


Figure 2. CDCLVD2102 Block Diagram



**PIN FUNCTIONS**

PIN		TYPE	DESCRIPTION	
NAME	NO.			
VCC	5	Power	2.5V supplies for the device	
GND	1	Ground	Device ground	
INP0, INN0	6, 7	Input	Differential input pair or single ended input	
INP1, INN1	3, 4	Input	Differential redundant input pair or single ended input	
V <sub>AC_REF</sub>	8	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin	
OUTP0, OUTN0	9, 10	Output	Differential LVDS output pair no. 0	INP0/INN0 is the input
OUTP1, OUTN1	11, 12	Output	Differential LVDS output pair no. 1	
OUTP2, OUTN2	13, 14	Output	Differential LVDS output pair no. 2	INP1/INN1 is the input
OUTP3, OUTN3	15, 16	Output	Differential LVDS output pair no. 3	
EN	2	Input with internal 200kΩ pull-up and pull-down	Control pin – enables or disables the outputs, (See <a href="#">Table 1</a> )	
Thermal Pad			See thermal management recommendations	

**Table 1. Output Control Table**

EN	CLOCK OUTPUTS
0	All outputs disabled (static "0")
OPEN	All outputs enabled
1	OUT0, OUT1 enabled and OUT2, OUT3 disabled (static "0")

**ABSOLUTE MAXIMUM RATINGS**

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE / UNIT
Supply voltage range, V <sub>CC</sub>	–0.3 to 2.8 V
Input voltage, V <sub>I</sub>	–0.2 to (V <sub>CC</sub> + 0.2) V
Output voltage range, V <sub>O</sub>	–0.2 to (V <sub>CC</sub> + 0.2) V
Driver short circuit current, I <sub>OSD</sub>	See Note <sup>(2)</sup>
Electrostatic discharge (HBM, 1.5 kΩ, 100 pF)	>3000 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) The outputs can handle permanent short.

**RECOMMENDED OPERATING CONDITIONS**

	MIN	TYP	MAX	UNITS
Device supply voltage, V <sub>CC</sub>	2.375	2.5	2.625	V
Ambient temperature, T <sub>A</sub>	–40		85	°C

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		CDCLVD2102	UNITS
		RGT	
		16 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	51.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	85.4	
$\theta_{JB}$	Junction-to-board thermal resistance	20.1	
$\psi_{JT}$	Junction-to-top characterization parameter	1.3	
$\psi_{JB}$	Junction-to-board characterization parameter	19.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**ELECTRICAL CHARACTERISTICS:**

At  $V_{CC} = 2.375\text{ V}$  to  $2.625\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>EN PIN INPUT CHARACTERISTICS</b>					
$V_{dI3}$	3-State	Open	$0.5 \times V_{CC}$		V
$V_{dIH}$	Input high voltage		$0.7 \times V_{CC}$		V
$V_{dIL}$	Input low voltage			$0.2 \times V_{CC}$	V
$I_{dIH}$	Input high current	$V_{CC} = 2.625\text{ V}$ , $V_{IH} = 2.625\text{ V}$		30	$\mu\text{A}$
$I_{dIL}$	Input low current	$V_{CC} = 2.625\text{ V}$ , $V_{IL} = 0\text{ V}$		-30	$\mu\text{A}$
$R_{pull(EN)}$	Input pull-up/ pull-down resistor		200		k $\Omega$
<b>2.5V LVC MOS (see Figure 7) INPUT CHARACTERISTICS</b>					
$f_{IN}$	Input frequency			200	MHz
$V_{th}$	Input threshold voltage	External threshold voltage applied to complementary input	1.1	1.5	V
$V_{IH}$	Input high voltage		$V_{th} + 0.1$	$V_{CC}$	V
$V_{IL}$	Input low voltage		0	$V_{th} - 0.1$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625\text{ V}$ , $V_{IH} = 2.625\text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Input low current	$V_{CC} = 2.625\text{ V}$ , $V_{IL} = 0\text{ V}$		-10	$\mu\text{A}$
$\Delta V/\Delta T$	Input edge rate	20% – 80%	1.5		V/ns
$C_{IN}$	Input capacitance		2.5		pF
<b>DIFFERENTIAL INPUT CHARACTERISTICS</b>					
$f_{IN}$	Input frequency	Clock input		800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	$V_{ICM} = 1.25\text{ V}$	0.3	1.6	$V_{P-P}$
$V_{ICM}$	Input common-mode voltage range	$V_{IN, DIFF, PP} > 0.4\text{ V}$	1	$V_{CC} - 0.3$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625\text{ V}$ , $V_{IH} = 2.625\text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Input low current	$V_{CC} = 2.625\text{ V}$ , $V_{IL} = 0\text{ V}$		-10	$\mu\text{A}$
$\Delta V/\Delta T$	Input edge rate	20% to 80%	0.75		V/ns
$C_{IN}$	Input capacitance		2.5		pF

**ELECTRICAL CHARACTERISTICS: (continued)**

 At  $V_{CC} = 2.375\text{ V}$  to  $2.625\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVDS OUTPUT CHARACTERISTICS</b>						
$ V_{OD} $	Differential output voltage magnitude	$V_{IN, DIFF, PP} = 0.3\text{ V}, R_L = 100\ \Omega$	250		450	mV
$\Delta V_{OD}$	Change in differential output voltage magnitude		-15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP} = 0.6\text{ V}, R_L = 100\ \Omega$	-15		15	mV
$V_{ring}$	Output overshoot and undershoot	Percentage of output amplitude $V_{OD}$			10%	
$V_{OS}$	Output ac common mode	$V_{IN, DIFF, PP} = 0.6\text{ V}, R_L = 100\ \Omega$		25	70	mV <sub>PP</sub>
$I_{OS}$	Short-circuit output current	$V_{OD} = 0\text{ V}$			$\pm 24$	mA
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.3\text{ V}$		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK, O\_WB}$	Within bank output skew				15	ps
$t_{SK, O\_BB}$	Bank-to-bank output skew	Both inputs are phase aligned			100	ps
$t_{SK, P}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	Edge speed = $0.75\text{ V/ns}$ , 10 kHz – 20 MHz			0.3	ps, RMS
$t_R/t_F$	Output rise/fall time	20% to 80%, $100\ \Omega$ , 5 pF	50		300	ps
$I_{CCSTAT}$	Static supply current	Outputs unterminated, $f = 0\text{ Hz}$		27	45	mA
$I_{CC100}$	Supply current	All outputs enabled, $R_L = 100\ \Omega$ , $f = 100\text{ MHz}$		49	77	mA
$I_{CC800}$	Supply current	All outputs enabled, $R_L = 100\ \Omega$ , $f = 800\text{ MHz}$		76	106	mA
<b><math>V_{AC\_REF}</math> CHARACTERISTICS</b>						
$V_{AC\_REF}$	Reference output voltage	$V_{CC} = 2.5\text{ V}, I_{load} = 100\ \mu\text{A}$	1.1	1.25	1.35	V

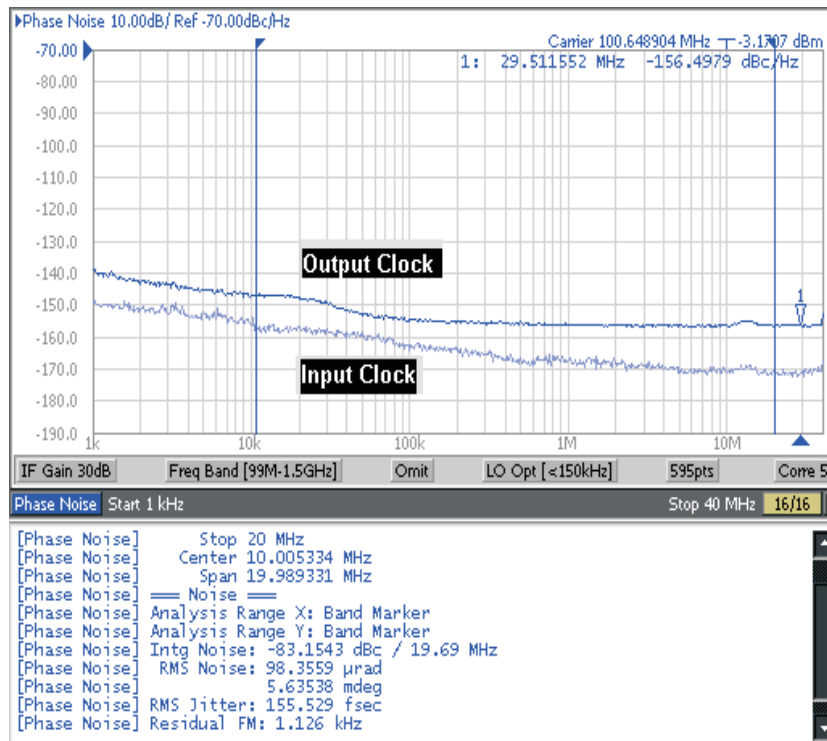
### Typical Additive Phase Noise Characteristics for 100 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

### Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

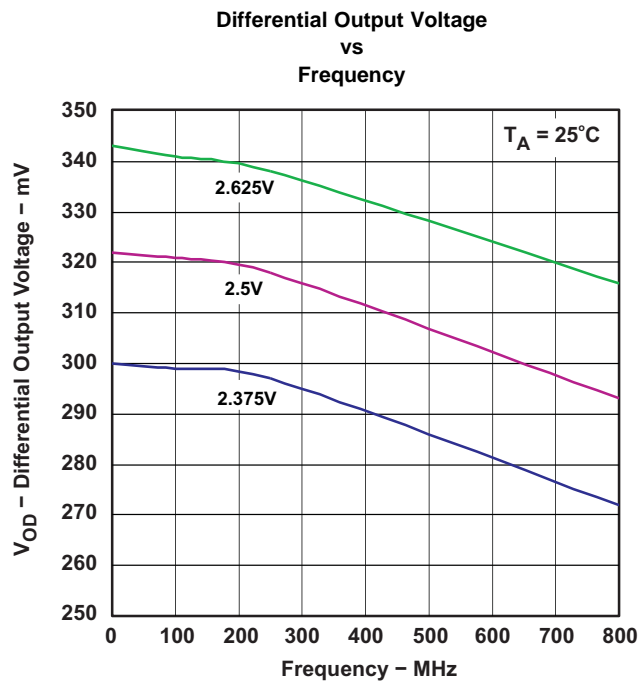
PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-138		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

**TYPICAL CHARACTERISTICS**  
**INPUT CLOCK AND OUTPUT CLOCK PHASE NOISES**  
 vs  
**FREQUENCY FROM THE CARRIER ( $T_A = 25^\circ\text{C}$  and  $V_{CC} = 2.5\text{V}$ )**



Input clock jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

**Figure 3. 100 MHz Input and Output Phase Noise Plot**



**Figure 4.**

TEST CONFIGURATIONS

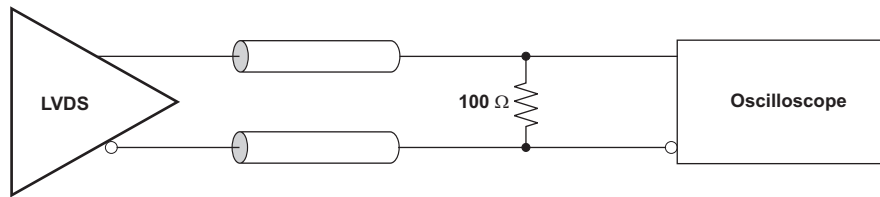


Figure 5. LVDS Output DC Configuration During Device Test

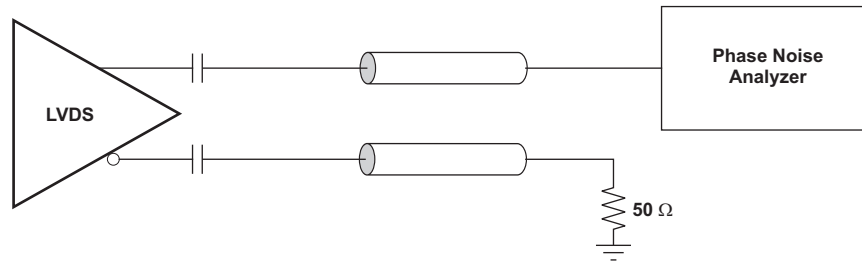


Figure 6. LVDS Output AC Configuration During Device Test

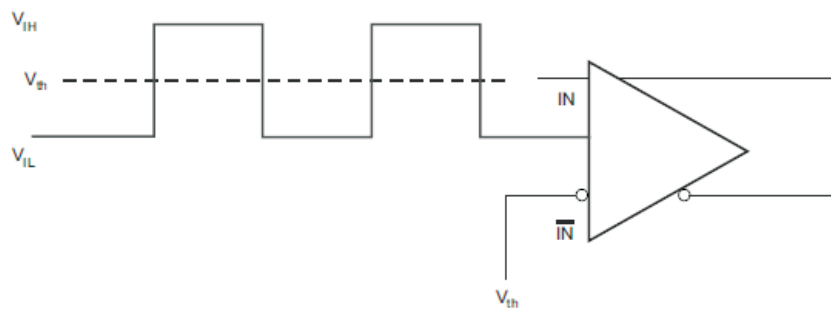


Figure 7. DC Coupled LVCMOS Input During Device Test

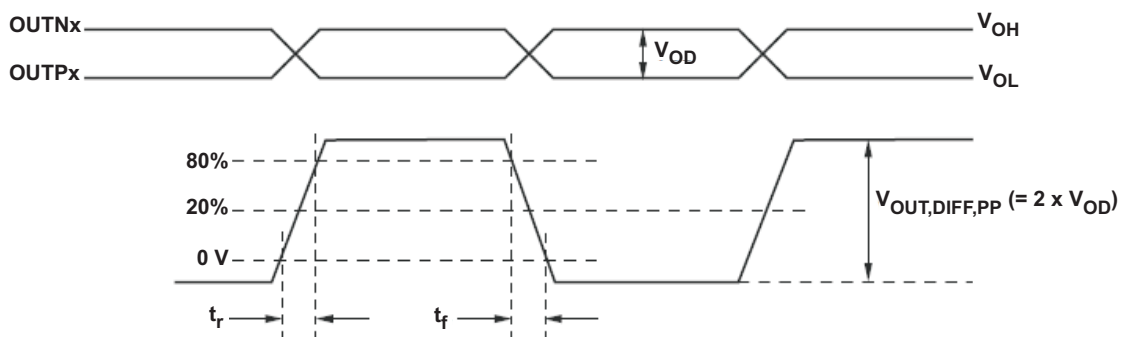
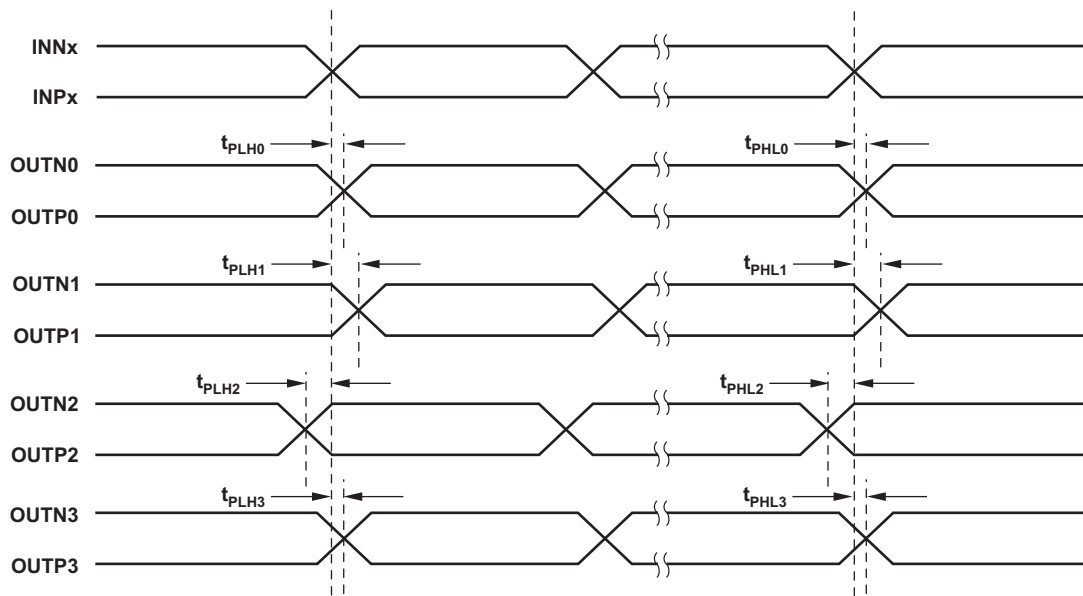


Figure 8. Output Voltage and Rise/Fall Time





- A. Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, 3$ ).
- B. Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  across multiple devices ( $n = 0, 1, 2, 3$ ).
- C. Both inputs ( $IN_0$  and  $IN_1$ ) are phase aligned.

Figure 9. Output Skew and Part-to-Part Skew

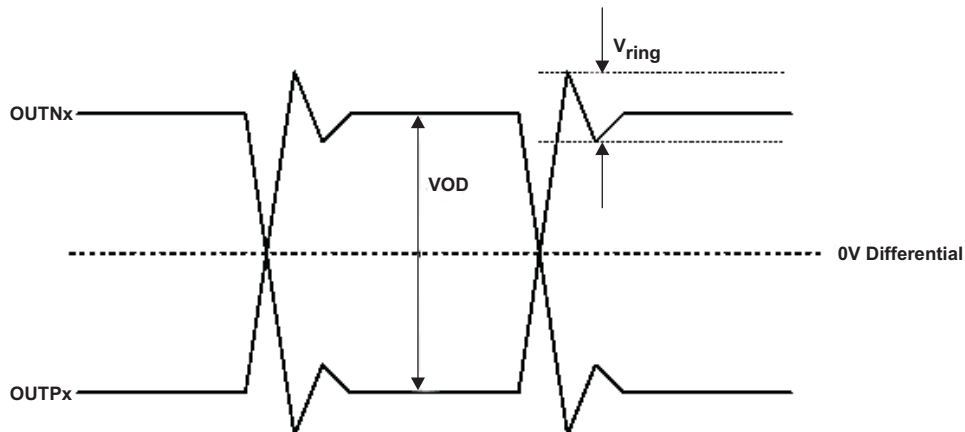


Figure 10. Output Overshoot and Undershoot

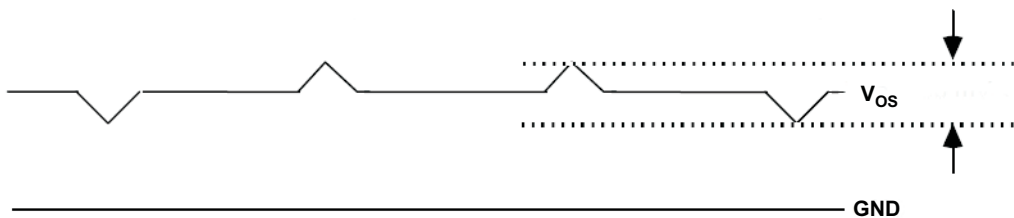


Figure 11. Output AC Common Mode

## APPLICATION INFORMATION

### THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The Thermal Pad must be soldered down to ensure adequate heat conduction to of the package. Figure 12 shows a recommended land and via pattern.

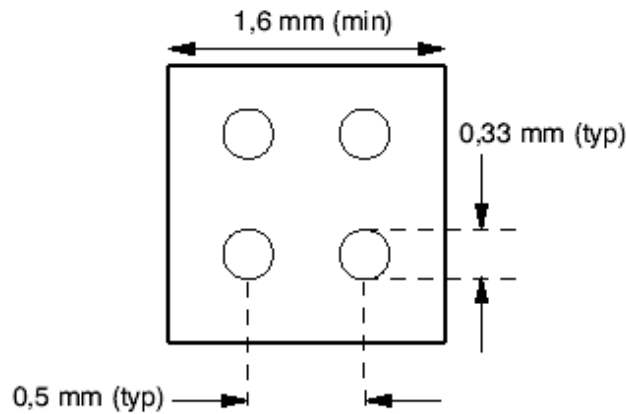


Figure 12. Recommended PCB Layout

### POWER-SUPPLY FILTERING

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1  $\mu\text{F}$ ) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

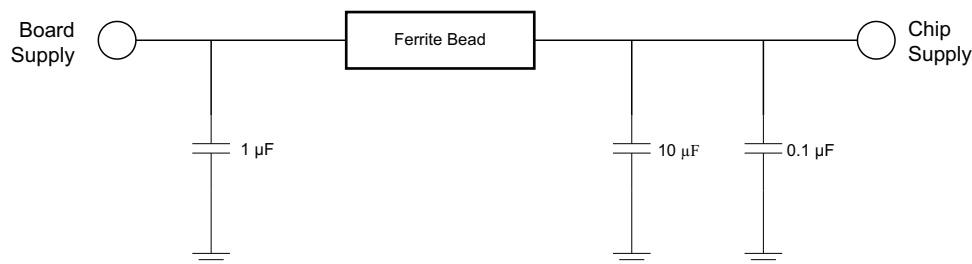


Figure 13. Power-Supply Decoupling

## LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD2102, ac-coupling should be used. If the LVDS receiver has internal 100 ohm termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.

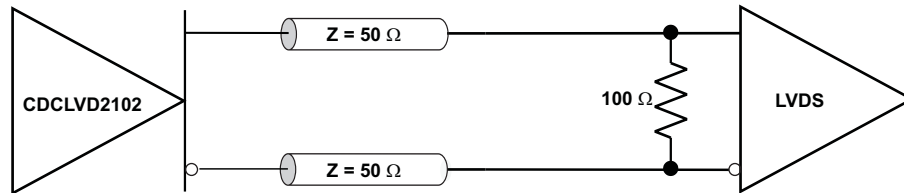


Figure 14. Output DC Termination

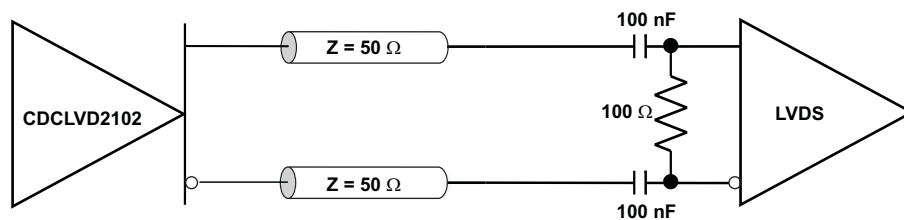


Figure 15. Output AC Termination With Receiver Internally Biased

## INPUT TERMINATION

The CDCLVD2102 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD2102 inputs with dc or ac coupling as shown [Figure 16](#) and [Figure 17](#), respectively.

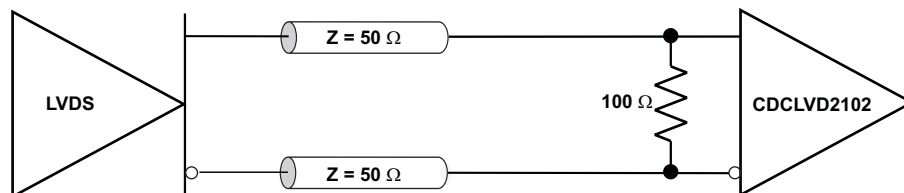


Figure 16. LVDS Clock Driver Connected to CDCLVD2102 Input (DC Coupled)

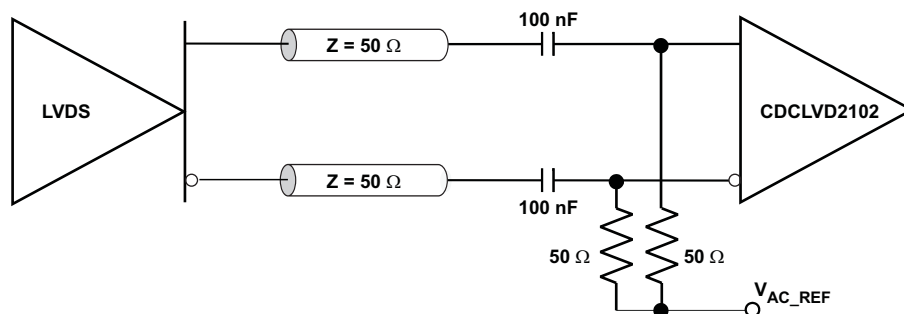


Figure 17. LVDS Clock Driver Connected to CDCLVD2102 Input (AC Coupled)

Figure 18 shows how to connect LVPECL inputs to the CDCLVD2102. The series resistors are required to reduce the LVPECL signal swing if the signal swing is  $>1.6 V_{PP}$ .

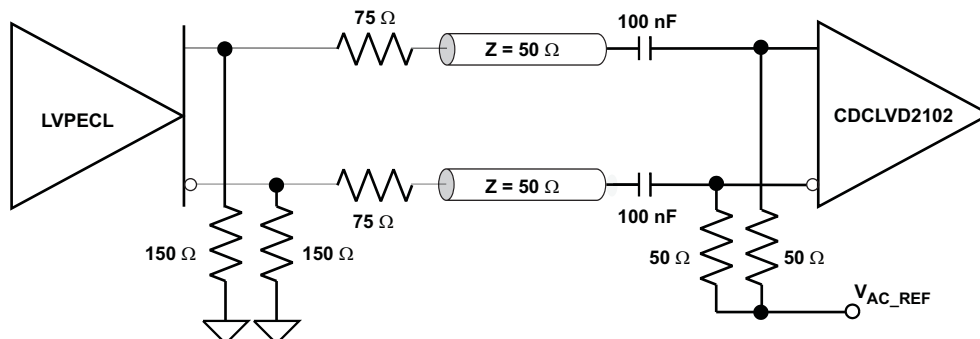


Figure 18. LVPECL Clock Driver Connected to CDCLVD2102 Input

Figure 19 illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD2102 directly. The series resistance ( $R_S$ ) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to  $V_{IH} \leq V_{CC}$ .

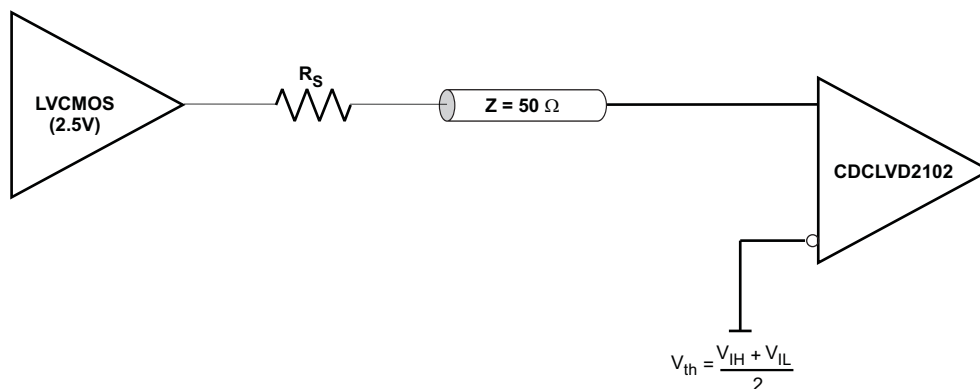


Figure 19. 2.5V LVCMOS Clock Driver Connected to CDCLVD2102 Input

If one of the buffers is used, then the other unused buffer should be disabled through the EN pin, and the unused input pins should be grounded by 1kΩ resistors.

## REVISION HISTORY

Changes from Original (May 2010) to Revision A	Page
• Changed Features bullet From: ESD Protection Exceeds 2kV HBM, 500V CDM To: ESD Protection Exceeds 3 kV HBM, 1 kV CDM .....	1
• Electrostatic discharge was <2000 .....	3
• $\Delta V_{OD}$ values, MIN was -50, MAX was 50 .....	5
• $V_{OC(SS)}$ MIN value was 1.125 .....	5
• $\Delta V_{OC(SS)}$ values, MIN was -50, MAX was 50 .....	5
• $V_{ring}$ MAX value was 20% .....	5
• $V_{OS}$ values, TYP was 30, MAX was 100 .....	5
• $t_{PD}$ MAX value was 2 .....	5
• $t_{SK, PP}$ - deleted the TYP value of 300 .....	5
• $t_R/t_F$ MIN value was 200 .....	5
• $I_{CCSTAT}$ MAX value was 42 .....	5
• Added new paragraph following <a href="#">Figure 19</a> .....	12

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CDCLVD2102RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
CDCLVD2102RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

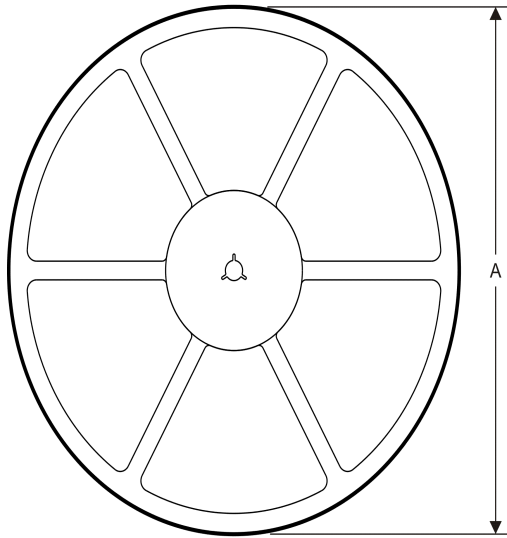
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD2102RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVD2102RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD2102RGTR	QFN	RGT	16	3000	338.1	338.1	20.6
CDCLVD2102RGTT	QFN	RGT	16	250	338.1	338.1	20.6



RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

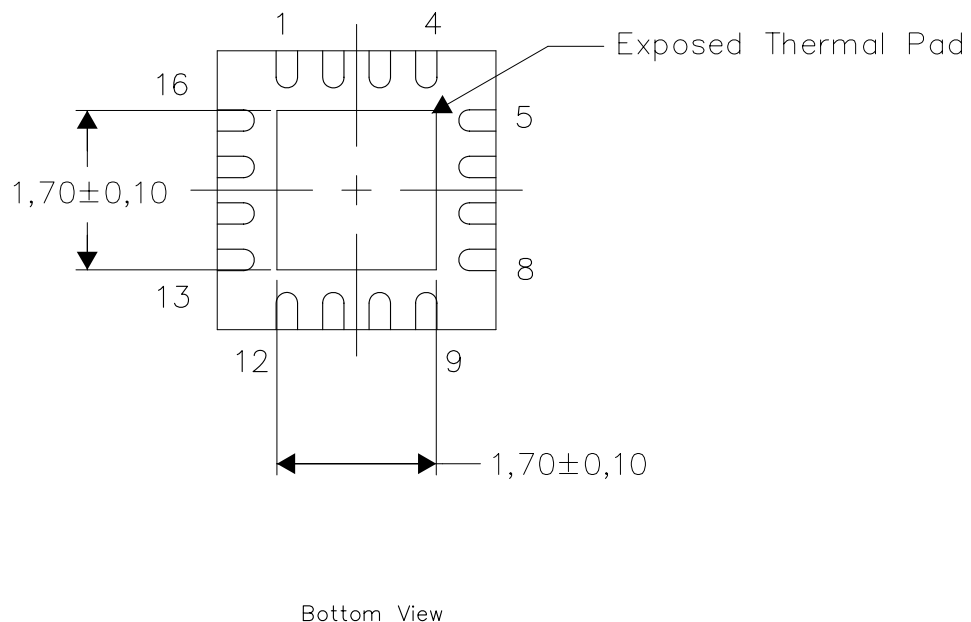
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



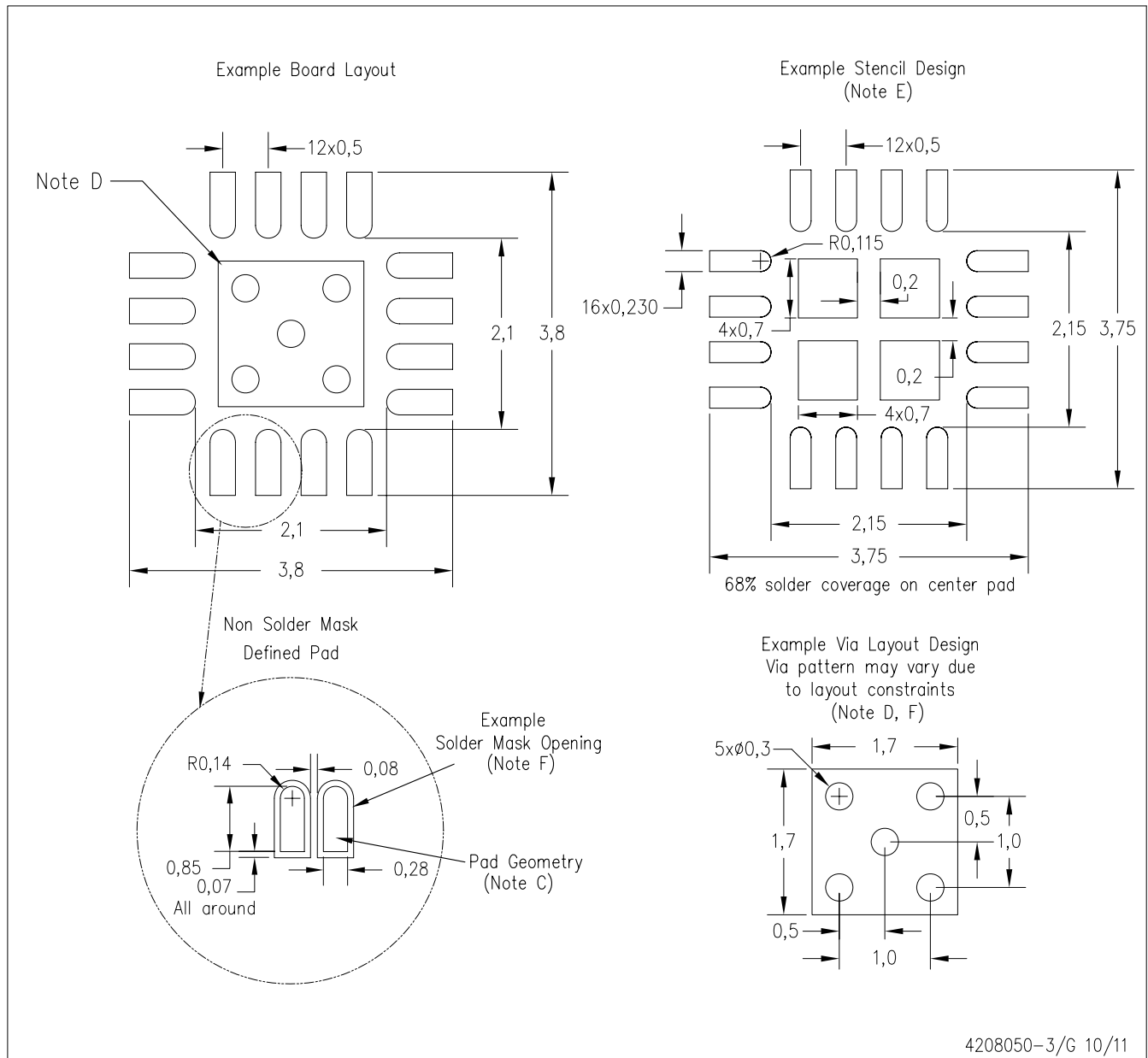
Exposed Thermal Pad Dimensions

4206349-4/Q 10/11

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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