TOPAZ SEMICONDUCTOR

CDG308, CDG309
CDG4308, CDG4309

QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCHES

ORDERING INFORMATION

Quad SPST Break-before-make	SO-16 Surface Mount Package		16-Pin Plastic DIP		16-Pin Ceramic DIP		20-Pin Plastic DIP	
Commercial Temp. Range	—	—	CDG308CJ	CDG309CJ	—	—	—	—
Industrial Temp. Range	—	—	CDG308BJ	CDG309BJ	CDG308BK	CDG309BK	CDG4308BJ	CDG4309BJ
Ext. Industrial Temp. Range	CDG308DY	CDG309DY	—	—	—	—	—	—
Military Temp. Range			—	—	CDG308AK	CDG309AK	—	—
Logic '0' ≤ 1.0V Logic '1' ≥ 4.5V	Logic '1' ON	Logic '1' OFF	Logic '1' ON	Logic '1' OFF	Logic '1' ON	Logic '1' OFF	Logic '1' ON	Logic '1' OFF

FEATURES

- High Off Isolation, 68dB @ 10MHz
- Low Insertion Loss, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Cross Talk, -80dB @ 10MHz
- CMOS Compatible Inputs
- Low 'OFF' Leakage
- Industry Standard Pin-Out, CDG308/309

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

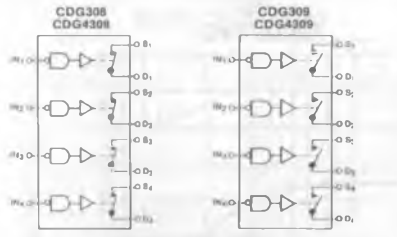
DESCRIPTION

Topaz Semiconductor CMOS/DMOS Analog Switches feature high-speed, low-power CMOS input logic and level translation circuitry and high-speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip. The CDG4308 and CDG4309 use the same die as CDG308 and CDG309; the extra isolating pin between switch input and output increases isolation by 6dB.

NOTE

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAMS

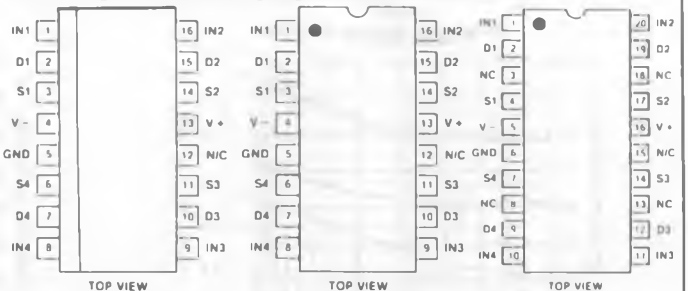


Four SPST Switches per Package
Switches Shown in Logic "1" Input Position

LOGIC TABLE

Logic	CDG308 CDG4308	CDG309 CDG4309
0	OFF	ON
1	ON	OFF

PIN CONFIGURATIONS



CDG308DY
CDG309DY
(See Package 21)

CDG308-309AK
CDG308-309BK
(See Package 15)

CDG308-309BJ
CDG308-309CJ
(See Package 10)

CDG4308BJ
CDG4309BJ
(See Package 12)

ABSOLUTE MAXIMUM RATINGS

V– Negative Supply Voltage ..... –20V
V+ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V– –0.3V
I_L Continuous Current, any Pin Except S or D ..... 20 mA
I_S Continuous Current, S or D ..... 30 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 180 mA
T_J Junction Temperature Range ..... –55 to +125°C
T_S Storage Temperature Range ..... –55 to +125°C
P_D Power Dissipation ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

V– Negative Supply Voltage ..... –8.0 to –15V
V+ Positive Supply Voltage ..... +8.0 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
V_S Analog Switch Voltage Range ..... –10 to +10V
T_{OP} Operating Temperature
(A Suffix) ..... –55 to +125°C
(B Suffix) ..... –25 to +85°C
(C Suffix) ..... 0 to +70°C
(D Suffix) ..... –40 to +85°C

ELECTRICAL CHARACTERISTICS (V– = –15V, V+ = +15V per channel unless otherwise noted, T_A = +25°C)

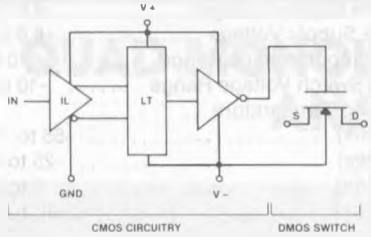
#	SYMBOL		PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	V_{ANALOG}	Analog Signal Range		–10		+10	V	
2		$r_{DS(on)}$	Switch ON Resistance			40	80	ohms	V_S = –10V
3						45	80		V_S = +2.0V
4						100	160		V_S = +10V
5		V_{IH}	High Level Input Voltage		4.5	3.4		V	
6		V_{IL}	Low Level Input Voltage				1.0		
7		I_{IN}	Logic Input Leakage Current			0.01	0.1	μA	V_{IN} = +5.0V
8						0.02	0.1		V_{IN} = +15V
9		$I_{D(off)}$	Switch OFF Leakage Current			0.2	5.0	nA	V_D = +10V, V_S = –10V; CDG309/4309
10		$I_{S(off)}$				0.4	5.0		V_S = +10V, V_D = –10V; V_{IN} = 5.0V
11		I–	Neg. Supply Quiescent Current			–0.1	–0.5	μA	CDG308/4308
12		I+	Pos. Supply Quiescent Current			0.1	0.5		V_{IN} = 1.0V
13	DYNAMIC	t_{on}	Switch Turn-On Time			140	250	nSec	V_{IN} = 1.0V CDG308, CDG4308
14		t_{off}	Switch Turn-Off Time			80	220		V_{IN} = 5.0V CDG309, CDG4309
15		O_{IRR}	Off Isolation	CDG308/309	60	62		dB	f = 10MHz
16			Rejection Ratio	CDG4308/4309	66	68			R_L = 50Ω
17		C_{CRR}	Cross-Coupling Rejection Ratio			80		dB	f = 10MHz, R_L = 50Ω
18		c_d	Drain-Node Capacitance			0.3		pF	V_{IN} = 1.0V CDG308, CDG4308
19		c_s	Source-Node Capacitance			3.0			V_{IN} = 5.0V, CDG309, CDG4309
									V_D = V_S = 0, f = 1MHz

ELECTRICAL CHARACTERISTICS (V– = –15V, V+ = +15V, per channel)

LIMITS AT TEMPERATURE EXTREMES

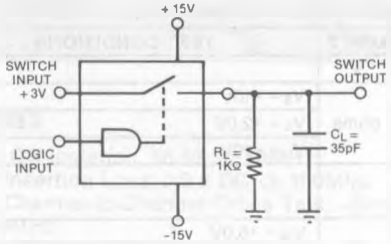
#	SYMBOL		PARAMETER	MAXIMUM @ T_A =					UNITS	TEST CONDITIONS
				–55°C	–25°C	+70°C	+85°C	+125°C		
1	STATIC	V_{ANALOG}	Analog Signal Range	±10	±10	±10	±10	±10	V	
2		$r_{DS(on)}$	Switch On Resistance	80	80	120	120	150	ohms	V_S = –10V
3				80	80	120	120	150		V_S = +2.0V
4				160	160	240	240	300		V_S = 10V
5		I_{IN}	Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	μA	V_{IN} = +5.0V
6				0.1	0.1	2.0	2.0	20		V_{IN} = +15V
7		$I_{D(OFF)}$	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V_D= +10V, V_S = –10V
8		$I_{S(OFF)}$		5.0	5.0	100	100	1000		V_S = +10V, V_D = –10V
9		I–	Supply Quiescent Currents	–0.5	–0.5	–20	–20	–100	μA	
10		I+		0.5	0.5	20	20	100		

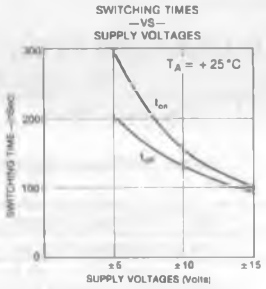
FUNCTIONAL DIAGRAM (1 of 4 channels)



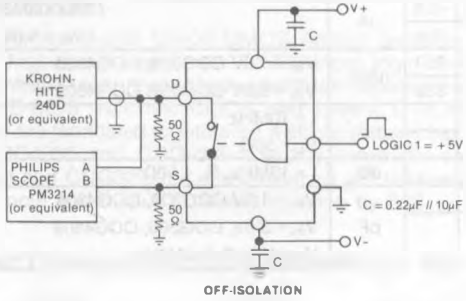
Switch Contacts:
Switches are bi-directional (Analog Input can be to Source or Drain). However, for optimum performance In Video Applications, connect Input to Source and Output to Drain.

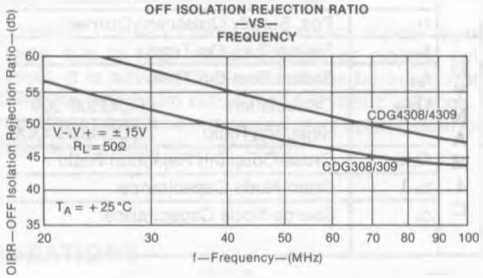
SWITCHING TIMES TEST CIRCUIT





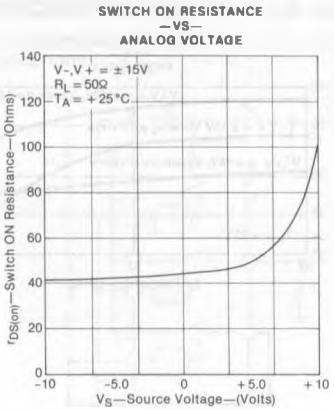
OFF ISOLATION TEST CIRCUIT

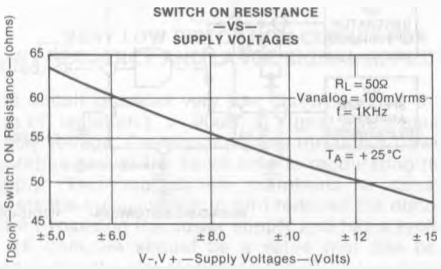




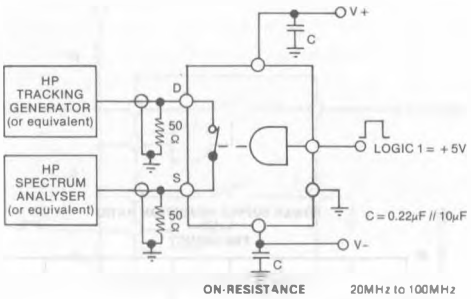
CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT

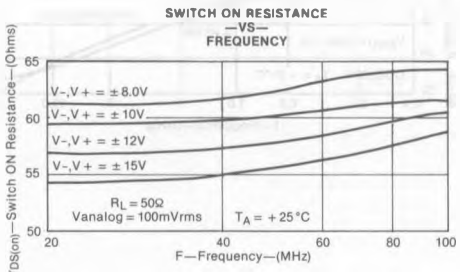
SWITCH ON RESISTANCE

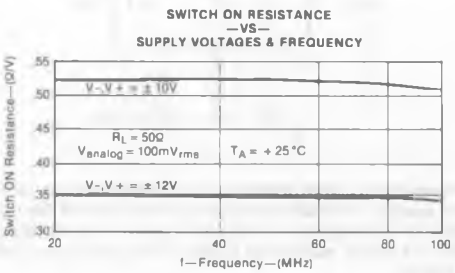




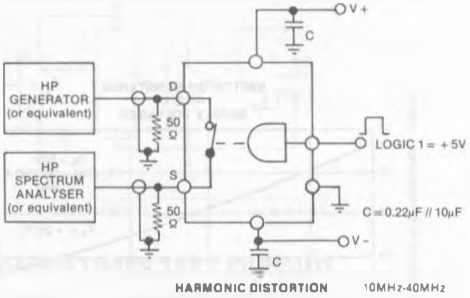
SWITCH ON RESISTANCE —VS— FREQUENCY TEST CIRCUIT



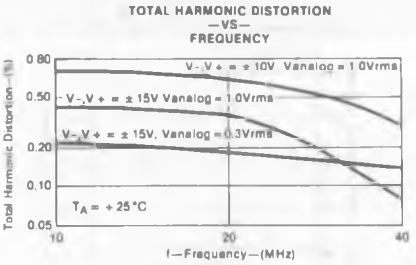


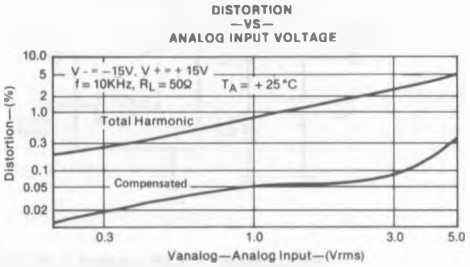


DISTORTION —VS— FREQUENCY

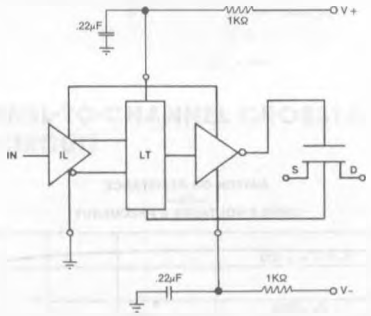


HARMONIC DISTORTION 10MHz-40MHz

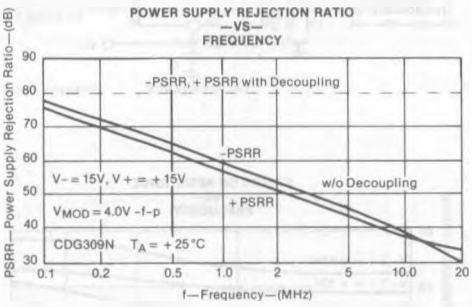




POWER SUPPLY REJECTION RATIO
POWER SUPPLY DECOUPLING CIRCUIT



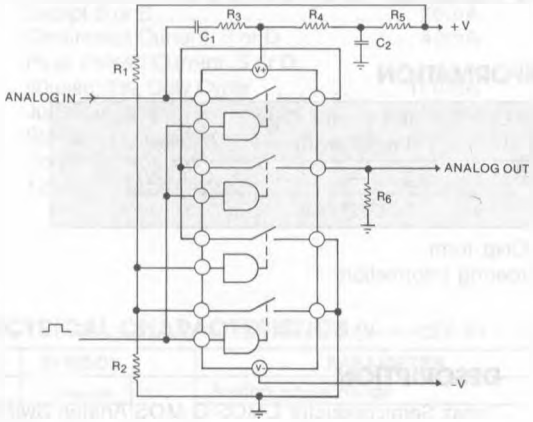
By inserting 1K ohm resistors in series with V+ and V- power supply lines and decoupling both pins at the device socket, it is possible to improve power supply rejection ratios of a video switch by 50dB at frequencies of 20MHz and higher.



APPLICATIONS

LOW DISTORTION, RAIL-TO-RAIL ANALOG SWITCH

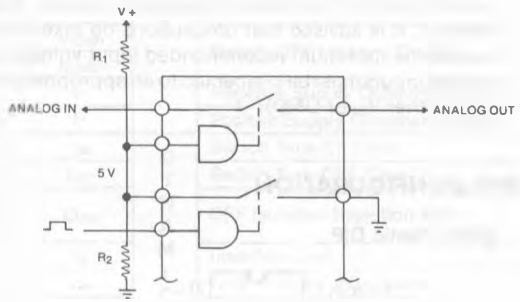
Features very low distortion for low frequency and large signal applications.



VERY LOW DISTORTION CIRCUIT FOR LOW FREQUENCY AND LARGE SIGNAL APPLICATIONS

This circuit provides very low distortion (< 0.1%) and high off isolation (> 90dB) at signal levels equal to the supply voltage. The signal passes through a T switch configuration and at the same time is modulating the power supply. This modulation maintains a constant on resistance $r_{DS(on)}$ which in turn reduces the distortion. R5 is for bypassing the power supply and has a typical value of 1K ohm, R4 should be a value that can be accommodated by the signal source as load, R3 is only necessary at loads lower than 100 ohms and should be selected during the initial design of the circuit, C1 has to be large enough for the lowest signal to pass and C2 will have to bypass all signals. R1 and R2 set up the one logic level for the control input and should be set to 5 volts.

LOGIC INVERTER



This circuit provides logic inversion with two resistors and one switch. It does not require additional logic parts. The resistors divide the supply voltage down to a 5 volt level when high and are switched to a low level via the switch. This configuration allows a single pole, single throw switch to be changed into a single pole, double throw switch.