

# CGS100P2530 PECL-TTL 1 to 10 Minimum Skew Clock Driver CGS100P2531 PECL-TTL 2 to 10 Minimum Skew Clock Driver

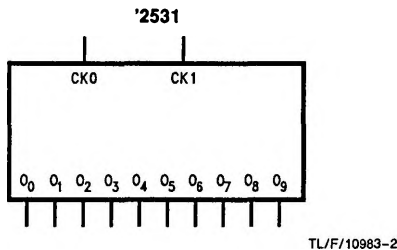
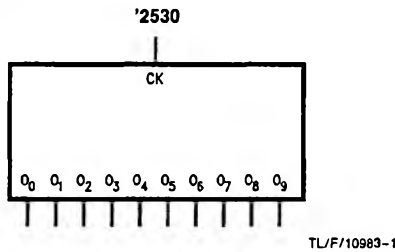
## General Description

These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications, particularly for ECL to TTL clock tree distribution schemes. The '2530 and '2531 are single supply devices with guaranteed minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2530 is a minimum skew clock driver with one input driving ten outputs and the '2531 is a selectable two input to 10 outputs, specifically designed for signal generation and clock distribution applications.

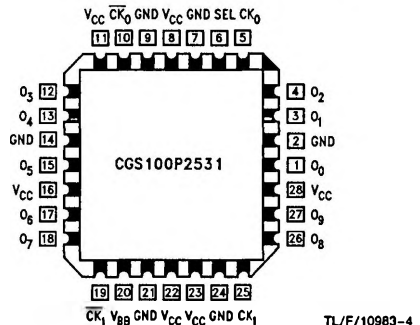
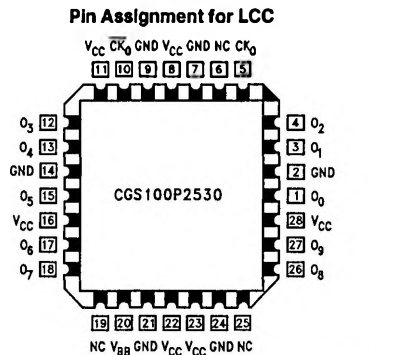
## Features

- PECL-TTL version of National's CGS74B2528 TTL clock drivers
- Clock Generation & Support (CGS) devices ideal for ECL and TTL clock trees with CGS 100311
- 1-to-10 or 2-to-10 low skew clock distribution
- 550 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- 28-pin PCC to minimize high speed switching noise and for low dynamic power consumption
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

## Logic Symbols



## Connection Diagrams



## Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CKn will have an active effect on the outputs of the circuit. When SEL = 1, the CK1 input is selected and when SEL = 0, the CK0 input is selected. The non-selected CKn input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK, CK1/CK0 pins when either the multiplexed ('2531) or the straight ('2530) clock distribution chip is selected.

## Truth Tables

'2530

Inputs		Outputs
CK	$\overline{CK}$	O <sub>0</sub> -O <sub>9</sub>
L	H	L
H	L	H
L	L	U
H	H	U
L	V <sub>BB</sub>	L*
H	V <sub>BB</sub>	H*
V <sub>BB</sub>	X	V <sub>BB</sub>

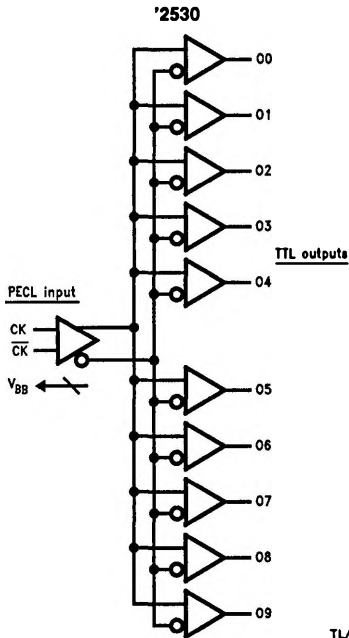
L = Low Logic Level  
 H = High Logic Level  
 X = Don't Care  
 U = Undefined  
 \* = Single Ended Operation

Pin Description

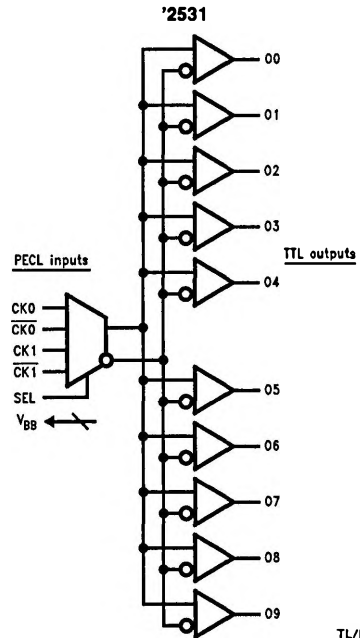
Pin Names	Description
CK	PECL Differential Clock Input ('2530)
CK0, CK1	PECL Differential Clock Input ('2531)
O <sub>0</sub> -O <sub>9</sub>	TTL Outputs
SEL	PECL Clock Select ('2531)

'2531

Inputs					Outputs
CK0	$\overline{CK0}$	CK1	$\overline{CK1}$	SEL	O <sub>0</sub> -O <sub>9</sub>
L	H	X	X	L	L
H	L	X	X	L	H
L	L	X	X	L	U
H	H	X	X	L	U
L	V <sub>BB</sub>	X	X	L	L*
H	V <sub>BB</sub>	X	X	L	H*
X	X	L	H	H	L
X	X	H	L	H	H
X	X	L	L	H	U
X	X	H	H	H	U
X	X	L	V <sub>BB</sub>	H	L*
X	X	H	V <sub>BB</sub>	H	H*



TL/F/10983-5



TL/F/10983-6

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature	
Plastic	150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
TTL Input Voltage (Note 2)	-0.5V to +7.0V
TTL Input Current (Note 2)	-30 mA to +5.0 mA
V <sub>BB</sub> Output Current	-5.0 mA to +1.0 mA
ECL Input Potential to GND Pin	-0.5V to V <sub>CC</sub> + 0.5V
Typical $\theta_{JA}$	V Package
0 LFM Airflow	69
225 LFM	53
500 LFM	45

Voltage Applied to Output  
(with V<sub>CC</sub> = 0V)

-0.5V to V<sub>CC</sub>

Current Applied to Output  
in Low State (Max)

Twice the Rated  
I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)

2000V

**Recommended Operating Conditions**

Operating Free Air Temperature  
Range

-40°C to +85°C

Supply Voltage

4.5V to 5.5V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Over recommended operating free air temperature range. All typical values are measured at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = -3 mA, V <sub>CC</sub> = 4.5V	2.4			V
		I <sub>OH</sub> = 48 mA, V <sub>CC</sub> = 4.5V	2.0			
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = 4.5V, I <sub>OL</sub> = 64 mA		0.375	0.55	V
V <sub>BB</sub>	Output Reference Voltage	I <sub>V<sub>BB</sub></sub> = -1 mA	V <sub>CC</sub> - 1.38		V <sub>CC</sub> - 1.26	V
V <sub>DIFF</sub>	Input Voltage Differential	Required for Full Output Swing	150			mV
V <sub>CM</sub>	Common Mode Voltage	High Level	V <sub>CC</sub> - 1.6		V <sub>CC</sub> - 0.4	V
V <sub>IH</sub>	Input High Voltage	Guarantee HIGH Signal for All Inputs	V <sub>CC</sub> - 1.165		V <sub>CC</sub> - 0.87	V
V <sub>IL</sub>	Input Low Voltage	Guarantee HIGH Signal for All Inputs	V <sub>CC</sub> - 1.83		V <sub>CC</sub> - 1.475	V
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> = V <sub>IL</sub> (min)	0.50			μA
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> = V <sub>IH</sub> (max)			50	μA
I <sub>CBO</sub>	Input Leakage Current	V <sub>IN</sub> = 0	-10			μA
I <sub>CCH</sub>	Supply Current	V <sub>CC</sub> = 5.5V	'2530		30	mA
			'2531		33	
I <sub>OS</sub>	Output Current Drive	V <sub>CC</sub> = 5.5V, V <sub>O</sub> = 2.25V	-50		-150	mA
I <sub>CCL</sub>	Supply Current	V <sub>CC</sub> = 5.5V	'2530		72	mA
			'2531		75	

## AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	CGS100P			Units
		$V_{CC} = 4.5V \text{ to } 5.5V$ $T_A = -40^\circ C \text{ to } +85^\circ C$ $C_L = 50 \text{ pF}$ $R_L = 500\Omega$			
		Min	Typ	Max	
$f_{MAX}$	Frequency Maximum	70			MHz
$t_{PLH}$	Low-to-High Propagation Delay CK to $O_n$ ('2530)	3.4	5.0	7.0	ns
$t_{PHL}$	High-to-Low Propagation Delay CK to $O_n$ ('2530)	3.4	5.0	7.0	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay CKn to $O_n$ ('2531)	4.0 4.0	5.0 5.0	8.0 8.0	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay SEL to $O_n$ ('2531)	5.0 5.0	5.0 5.0	10.0 10.0	ns

## Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

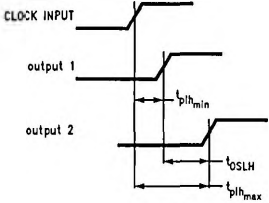
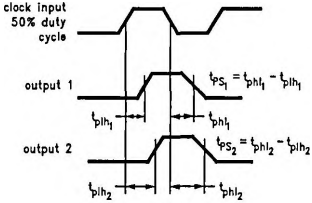
Symbol	Parameter	$V_{CC}$ (V)*	CGS100P			Units
			$T_A = -40^\circ C \text{ to } +85^\circ C$ $C_L = 50 \text{ pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150 550	ps	
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.5		150 550	ps	
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6 1.1	ns	
$t_{rise}$ , $t_{fall}$	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	5.0		1.0 1.5	ns	

\*Voltage Range 5.0 is  $5.0V \pm 0.5V$

**Note 1:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ) or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design. See Figures A and B of Parameter Measurement Information.

# Minimum Skew Parameters

## Parameter Measurement Information (Preliminary)

Definition	Example	Significance
<p><b><math>t_{OSHL}, t_{OSLH}</math></b></p> <p><b>Common Edge Skew:</b></p> <p>Output Skew for HIGH-to-LOW Transitions:  <math>t_{OSHL} =  t_{PHL_{max}} - t_{PHL_{min}} </math></p> <p>Output Skew for LOW-to-HIGH Transitions:  <math>t_{OSLH} =  t_{PLH_{max}} - t_{PLH_{min}} </math></p> <p>Propagation delays are measured across the outputs of any given device.</p>	 <p>The diagram shows a clock input signal that transitions from low to high. Two output signals, output 1 and output 2, follow. Output 1 has a shorter propagation delay than output 2. The minimum propagation delay for the high-to-low transition is labeled <math>t_{PHL_{min}}</math> and the maximum is <math>t_{PHL_{max}}</math>. Similarly, the minimum propagation delay for the low-to-high transition is labeled <math>t_{PLH_{min}}</math> and the maximum is <math>t_{PLH_{max}}</math>. The output skew for high-to-low transitions is <math>t_{OSHL}</math> and for low-to-high transitions is <math>t_{OSLH}</math>.</p> <p><b>FIGURE A</b></p>	<ul style="list-style-type: none"> <li>• <math>t_{OS}</math>, Output Skew or Common Edge Skew</li> <li>• Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.</li> </ul>
<p><b><math>t_{PS}</math></b></p> <p><b>Pin Skew or Transition Skew:</b></p> <p><math>t_{PS} =  t_{PHL_i} - t_{PLH_i} </math></p> <p>Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. <math>t_{PS}</math> is the maximum difference for outputs <math>i = 1</math> to 8 within a device package.</p>	 <p>The diagram shows a clock input signal with a 50% duty cycle. Two output signals, output 1 and output 2, follow. For output 1, the propagation delay for the high-to-low transition is <math>t_{PHL_1}</math> and for the low-to-high transition is <math>t_{PLH_1}</math>. The transition skew for output 1 is <math>t_{PS_1} = t_{PHL_1} - t_{PLH_1}</math>. For output 2, the propagation delay for the high-to-low transition is <math>t_{PHL_2}</math> and for the low-to-high transition is <math>t_{PLH_2}</math>. The transition skew for output 2 is <math>t_{PS_2} = t_{PHL_2} - t_{PLH_2}</math>.</p> <p><b>FIGURE B</b></p>	<ul style="list-style-type: none"> <li>• <math>t_{PS}</math>, Pin Skew or Transition Skew</li> <li>• Skew parameter to observe duty cycle degradation of any output signal (pin).</li> </ul>