National Semiconductor

**PRELIMINARY**

# CMOS Crystal Clock Generators CGS3311/CGS3312/CGS3313/CGS3314/CGS3315/ CGS3316/CGS3317/CGS3318/CGS3319

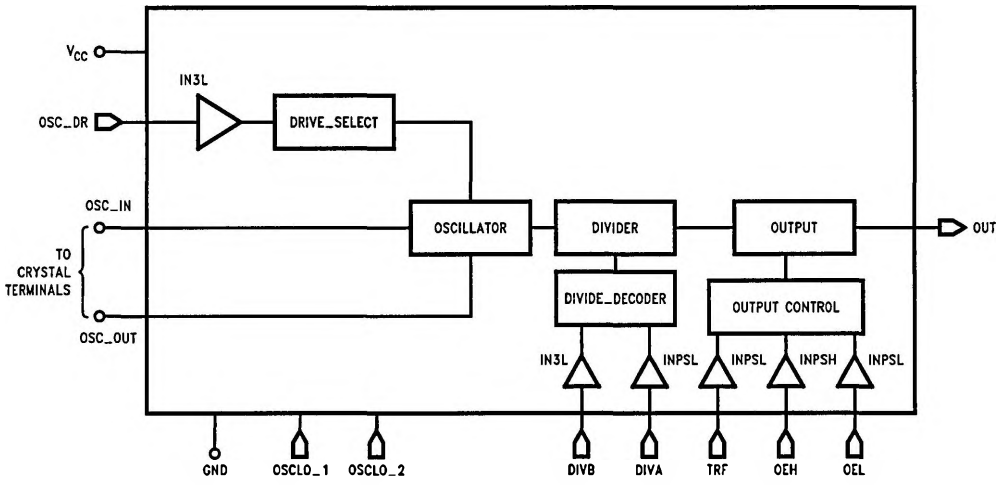
## General Description

These devices are designed for Clock Generation and Support (CGS™) applications up to 110 MHz. The CGS331x series of devices are crystal controlled CMOS oscillators requiring a minimum of external components. The 331x devices provide selectable output divide ratio (and selectable crystal drive level). The circuit is designed to operate over a wide frequency range using fundamental model or overtone crystals.

## Features

- National's CGS™ family of devices for high frequency clock source applications
- Crystal frequency operation range:
  fundamental: 10 MHz to 100 MHz typical
  3rd or 5th overtone: 10 MHz to 85 MHz
- Programmable oscillator drive
- Selectable fast output edge rates
- Output symmetry circuit to adjust 50% duty cycle point between CMOS and TTL levels
- Output current drive of 48 mA for $I_{OL}/I_{OH}$
- FACT™ CMOS output levels
- Output has high speed short circuit protection
- Basic oscillator type: Pierce
- Hysteresis inputs to improve noise margin

## Block Diagrams

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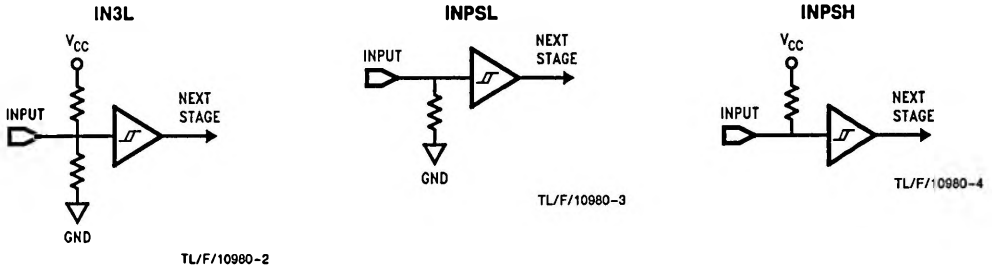
**Note:** Pin numbers vary for each device

## Block Diagrams (Continued)

### Input Drivers

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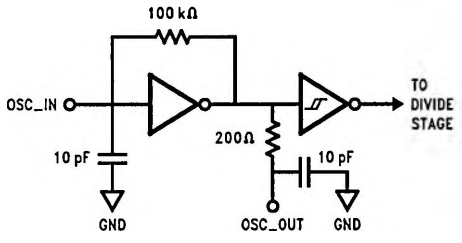
### Oscillator Stage

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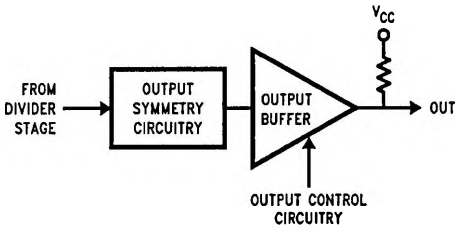
### Output Stage

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## Functional Description

**Summary of Device Options**

| Device | Divide | Enable | Drive | Output Rise/ Fall Time (ns) |
|---|---|---|---|---|
| 3311 | 1, 2, 4 | OEH | L, M, H | 2, 4 |
| 3312 | 1, 2, 4 | OEH | H | 2, 4 |
| 3313 | 8, 16, 32 | OEH | H | 4 |
| 3314 | 8, 16, 32 | OEH | L, M, H | 4 |
| 3315 | 1, 2, 4 | OEL | H | 1, 2 |
| 3316 | 4 | OEH | H | 4 |
| 3317 | 32 | OEH | H | 4 |
| 3318 | 1, 2, 4 | OEH | H | 1, 2 |
| 3319 | 1, 2, 4 | OEL | L, M, H | 2, 4 |

Each drive has one output with the choices of selecting frequency divide, output enable, crystal drive and output rise and fall time. Crystal drive options are:

L = Low Drive
M = Medium Drive
H = High Drive

## Pin Descriptions

**Note:** Pin out varies for each device.

OSC_IN Input to Oscillator Inverter. The output of the crystal would be connected here.

OSC_OUT Resistive Buffered Output of the Oscillator Inverter

OSC_DR 3 Level input pin that selects Oscillator Drive Level

DIVA Input used to select Binary Divide-by Option. This pin has CMOS compatible input levels.

DIVB 3 Level input used to select Binary Divide-by value.

OEH Active High TRI-STATE® enable pin. This pin pulls to a high value when left floating and TRI-STATEs the output when forced low. This pin has TTL compatible input levels.

OEL Active Low TRI-STATE enable pin. This pin pulls to a low value when left floating and TRI-STATES the output when forced high. This pin has TTL compatible input levels.

TRF Rise and Fall time override pin. Available only for die form.

OUT This pin is the main clock output on the device.

OSCLO_1 The Oscillator Low pin is the ground for the Oscillator.

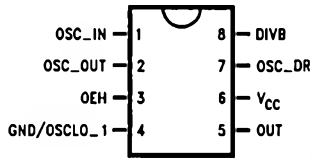
OSCLO_2 This pin is the same signal as OSCLO_1. It has been provided as an alternate connection for OSCLO_1 for hybrid assemblies.

$V_{CC}$ The power pin for the chip.

GND The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

## Connection Diagrams

**Pin Assignment for SOIC**

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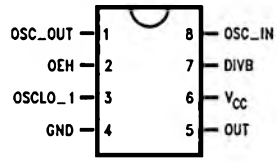
**(A) 3311**

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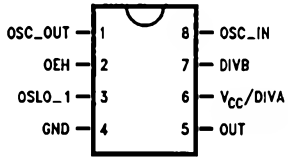
**(B) 3312**

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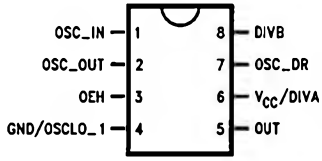
**(C) 3313**

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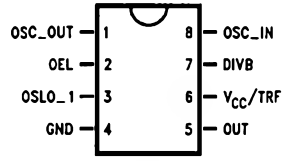
**(D) 3314**

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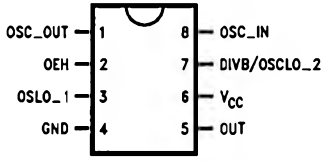
**(E) 3315**

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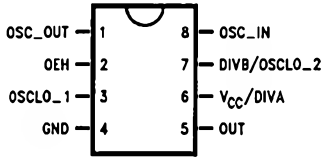
**(F) 3316**

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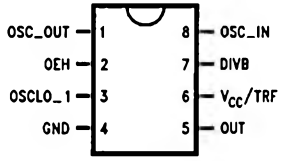
**(G) 3317**

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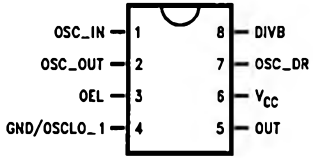
**(H) 3318**

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**(I) 3319**

## Truth Tables

**Division Selection**

| DIVB | DIVA | OEL | OEH | Divider Output |
|---|---|---|---|---|
| F | 0/F | X | X | Divide-by 1 |
| 1 | 0/F | 0 | 1 | Divide-by 2 |
| 0 | 0/F | 0 | 1 | Divide-by 4 |
| F | 1 | 0 | 1 | Divide-by 8 |
| 1 | 1 | 0 | 1 | Divide-by 16 |
| 0 | 1 | 0 | 1 | Divide-by 32 |
| X | X | 1 | X | Output Reset High at Re-enable |
| X | X | X | 0 | Output Reset High at Re-enable |

**Note:** Actual value of the floating OSC__DR and DIVB input is $V_{CC/2}$

**Rise and Fall Time Selection**

| OSC__DR | DIV | TRF | Rise/Fall Time (ns) |
|---|---|---|---|
| F | N | 0/F | 2 |
| F | N | 1 | less than 2 |
| F | Y | 0/F | 4 |
| F | Y | 1 | 2 |
| 0, 1 | X | 0/F | 4 |
| 0, 1 | X | 1 | 2 |

**Drive Selection**

| OSC__DR | Drive |
|---|---|
| 0 | Low |
| 1 | Medium |
| F | High |

**Note:** Where "F" indicates floating the input.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to 7.0V |
| DC Input Voltage Diode Current ($I_{IK}$) | ± 9mA |
| DC Input Voltage ($V_I$) | −0.5V to 7.0V |
| DC Output Diode Current ($I_{OK}$) | ±20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±70 mA |
| Storage Temperature ($T_{STG}$) | −55°C to +150°C |
| Junction Temperature ($T_J$) SOIC | 140°C/W |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to 5.5V |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ V |
| Operating Temperature ($T_A$) | −40°C to +85°C |

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | CGS3311 to 3319 | | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C | | $T_A$ = −40°C to +85°C | | $T_A$ = −55°C to +125°C | | | | |
| | | | Typ | Guaranteed Limits | | | | | | | |
| | | | | Min | Max | Min | Max | Min | Max | | |
| $V_{IH_{TTL}}$ | Minimum High Level Input Voltage. TTL Level Inputs (OEH, OEL) | 4.5<br>5.5 | | 2.0<br>2.0 | | 2.0<br>2.0 | | | | V | |
| $V_{IL_{TTL}}$ | Maximum Low Level Input Voltage. TTL Level Inputs (OEH, OEL) | 4.5<br>5.5 | | | 0.8<br>0.8 | | 0.8<br>0.8 | | | V | |
| $V_{IH_{CMOS}}$ | Minimum High Level Input Voltage. CMOS Level Inputs (DIVA) | 4.5<br>5.5 | | 3.15<br>3.85 | | 3.15<br>3.85 | | | | V | |
| $V_{IL_{CMOS}}$ | Maximum Low Level Input Voltage. CMOS Level Inputs (DIVA) | 4.5<br>5.5 | | | 1.35<br>1.65 | | 1.35<br>1.65 | | | V | |
| $V_{IN3L\_H}$ | Minimum Logic 1 Input for Three Level Input (DIVB, OSC_DR) | 4.5<br>5.5 | | 4.05<br>4.95 | | 4.05<br>4.95 | | | | V | |
| $V_{IN3L\_1/2}$ | Minimum Logic 1/2 Input for Three Level Input (DIVB, OSC_DR) | 4.5<br>5.5 | | 1.8<br>2.2 | 2.7<br>3.3 | 1.8<br>2.2 | 2.7<br>3.3 | | | V | |
| $V_{IN3L\_L}$ | Maximum Logic 0 Input Level Three Level Input (DIVB, OSC_DR) | 4.5<br>5.5 | | | 0.45<br>0.45 | | 0.45<br>0.45 | | | V | |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.40<br>5.40 | | 4.40<br>5.40 | | | | V | $I_{OUT}$ = −50 μA |
| | | 4.5<br>5.5 | | 3.86<br>4.86 | | 3.76<br>4.76 | | | | | $I_{OH}$ = −48 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IH}$ |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | CGS3311 to 3319 | | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | $T_A$ = −55°C to +125°C | | | |
| | | | Typ | Guaranteed Limits | | | | | | | |
| | | | | Min | Max | Min | Max | Min | Max | | |
| $V_{OL}$ | Minimum Low Level Output Voltage | 4.5 | 0.001 | | 0.1 | | 0.1 | | | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | | 0.1 | | 0.1 | | | | |
| | | 4.5 | | | 0.44 | | 0.44 | | | | $I_{OL}$ = +48 mA<br>$V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 5.5 | | | 0.44 | | 0.44 | | | | |
| $I_{IH_{RES}}$ | Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic High) | 5.5 | | 220 | 360 | 200 | 380 | | | μA | $V_{IN}$ = 5.5V |
| $I_{IL_{RES}}$ | Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic Low) | 5.5 | | −220 | −360 | −200 | −380 | | | μA | $V_{IN}$ = 0.0V |
| $I_{IH_{ENAB}}$ | Input Current for Enable Pin OEL | 5.5 | | 90 | 160 | 85 | 175 | | | μA | $V_{IN}$ = 5.5V |
| $I_{IL_{ENAB}}$ | Input Current for Enable pin OEH | 5.5 | | −90 | −160 | −85 | −175 | | | μA | $V_{IN}$ = 0.0V |
| $I_{IH_{OSC}}$ | Input Current for OSC_IN pin (Indicates Bias Resistance) | 5.5 | | 20 | 100 | 20 | 125 | | | μA | $V_{IN}$ = 5.5V |
| $I_{IL_{OSC}}$ | Input Current for OSC_IN pin (Indicates Bias Resistance) | 5.5 | | −20 | −100 | −20 | −125 | | | μA | $V_{IN}$ = 0.0V |
| $I_{OZH}$ | Output Disabled Current (Output High) | 4.5 | | | 3.0 | | 5.0 | | | μA | $V_{OUT}$ = $V_{CC}$ |
| | | 5.5 | | | 3.0 | | 5.0 | | | | |
| $I_{OZL}$ | Output Disabled Current (Output Low) | 4.5 | | | −140 | | −150 | | | μA | $V_{OUT}$ = 0.0V |
| | | 5.5 | | | −170 | | −180 | | | | |
| $I_{OLD}$ | Minimum Dynamic Output Current | 5.5 | | 75 | | 75 | | | | mA | $V_{OLD}$ = 1.65V |
| $I_{OHD}$ | Minimum Dynamic Output Current | 5.5 | | −75 | | −75 | | | | mA | $V_{OHD}$ = 3.85V |
| $I_{CC_{OSC\_L}}$ | Additional $I_{CC}$ with OSC_IN Floating. Low Drive Mode | 4.5 | | 0.6 | | 0.6 | | | | mA | OSC_IN = Float |
| | | 5.5 | | | 6.5 | | 6.5 | | | | |
| $I_{CC_{OSC\_M}}$ | Additional $I_{CC}$ with OSC_IN Floating. Low Drive Mode | 4.5 | | 1.7 | | 1.7 | | | | mA | OSC_IN = Float |
| | | 5.5 | | | 12.4 | | 12.4 | | | | |
| $I_{CC_{OSC\_H}}$ | Additional $I_{CC}$ with OSC_IN Floating. Low Drive Mode | 4.5 | | 5.5 | | 5.5 | | | | mA | OSC_IN = Float |
| | | 5.5 | | | 31.5 | | 31.5 | | | | |
| $I_{CC_T}$ | Additional Maximum $I_{CC}$ per Input (OEH, OEL Pins) | 5.5 | | | 1.5 | | 1.5 | | | mA | $V_{IN}$ = $V_{CC}$ − 2.1V |
| $I_{CC_{3L}}$ | Additional Maximum $I_{CC}$ per Input (DIVB, OSC_DR Inputs) | 5.5 | | | 1.5 | | 1.5 | | | mA | DIVB, OSC_DR Inputs Equal to $V_{CC/2}$ |

## AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

| Symbol | Parameter | $V_{CC}$* (V) | CGS331X | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | | $T_A$ = −55°C to +125°C, $C_L$ = 50 pF | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Frequency Maximum | 5.0 | 100 | | | | | | MHz |
| $t_{PZH}$ | Output High Enable Time | 5.0 | 1.0 | | 31.5 | | | | ns |
| $t_{PZL}$ | Output Low Enable Time | 5.0 | 1.0 | | 28.0 | | | | ns |
| $t_{PHZ}$ | Output High Disable Time | 5.0 | 1.0 | | 21.5 | | | | ns |
| $t_{PLZ}$ | Output Low Disable Time | 5.0 | 1.0 | | 16.0 | | | | ns |
| $t_{rise}$, $t_{fall}$ | Rise/Fall Time 30 pF, 20% to 80%) | 5.0 | | 4.0 | | | | | ns |

* Voltage Range 5.0 is 5.0V ± 0.5V