National Semiconductor

CGS74B303 Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation and Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

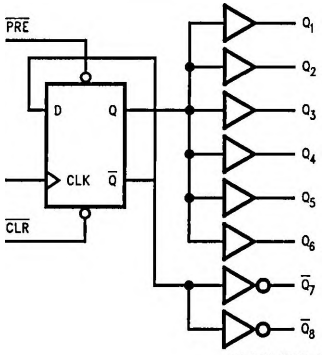
The CGS74B303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set Q and $\overline{Q}$ outputs high or low independent of CLK pin.

Features

- Clock Generation and Support (CGS) Devices ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST™ LSI process
- 1 ns pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Diagram



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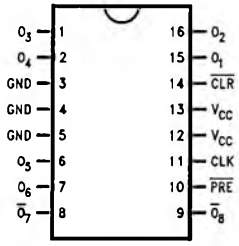
Connection Diagrams

Pin Assignment for DIP and SOIC



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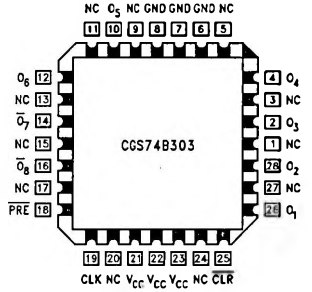
Pin Assignment for 28-Pin PCC



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Pin Description

Pin Names	Description
CLK	Clock Input
O_1–O_8	Outputs
$\overline{PRE}$	Preset
$\overline{CLR}$	Clear

Truth Table

Inputs			Outputs	
$\overline{CLR}$	$\overline{PRE}$	CLK	O_1–O_5	$\overline{O_7}$–$\overline{O_8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L*	L*
H	H	↑	$\overline{Q}$	Q
H	H	L	Q	$\overline{Q}$

*This state will not persist when $\overline{CLR}/\overline{PRE}$ returns to high.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})				7.0V	
Input Voltage (V_I)				7.0V	
Operating Free	74B303			0°C to +70°C	
Air Temperature	64B303			−40°C to +85°C	
Storage Temperature Range				−65°C to +150°C	
Typical θ_{JA}				303/304/305	
Airflow (LFM)	0	225	500		
Plastic (N) Package	95	70	60	°C/W	
Jedec SOIC (M) Package	118	96	86	°C/W	
PCC (V) Package	69	53	45	°C/W	

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−24 mA
Low Level Output Current (I_{OL})	48 mA
Free Air Operating Temperature (T_A)	0 to 70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics CGS74/64B303/304/305

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V		V_{CC} − 2			V
		I_{OH} = 24 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 48 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	m A
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1	−0.50	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current 303	V_{CC} = 5.5V	Outputs High		27	60	mA
			Outputs Low		45	60	mA
I_{CC}	Supply Current 304	V_{CC} = 5.5V	Outputs High		20	30	mA
			Outputs Low		42	55	mA
I_{CC}	Supply Current 305	V_{CC} = 5.5V	Outputs High		35	45	mA
			Outputs Low		42	55	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		CGS74B303 V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B303 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency		110			100			MHz
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n	M, N	4		8	4		8	ns
		V	4		8.5	4		9	
t_{PLH}, t_{PHL}	Propagation Delay PRE/CLR		3		12	3		12	ns
t_{SU}	Set Up Time before CLK		5			5			ns
t_W	CLK HI		4			4			ns
	CLK LO		4			4			
	CLR/PRE		4			4			

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		V_{CC}* (V)	CGS74B303 V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B303 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
				Min	Typ	Max	Min	Typ	Max	
t_{OSHL} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	1.0		0.5	1.0	ns
t_{OSLH} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	1.0		0.5	1.0	ns
t_{OSHL} $\overline{Q}$	Maximum Skew Common Edge	M, N	5.0		0.3	0.6		0.3	0.6	ns
	Output-to-Output Variation (Note 1)	V			0.3	0.75		0.3	0.75	
t_{OSLH} $\overline{Q}$	Maximum Skew Common Edge	M, N	5.0		0.3	0.6		0.3	0.6	ns
	Output-to-Output Variation (Note 1)	V			0.3	0.75		0.3	0.75	
$t_{OSLH/HL}$ Q,$\overline{Q}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		1.0	1.6		1.0	1.75	ns
t_{PS} Q	Maximum Skew Pin (Signal) Transition Variation (Note 1)		5.0			1.0			1.2	ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads		5.0		1.1 0.9	2.0 2.0		1.1 0.9	2.0 2.0	ns

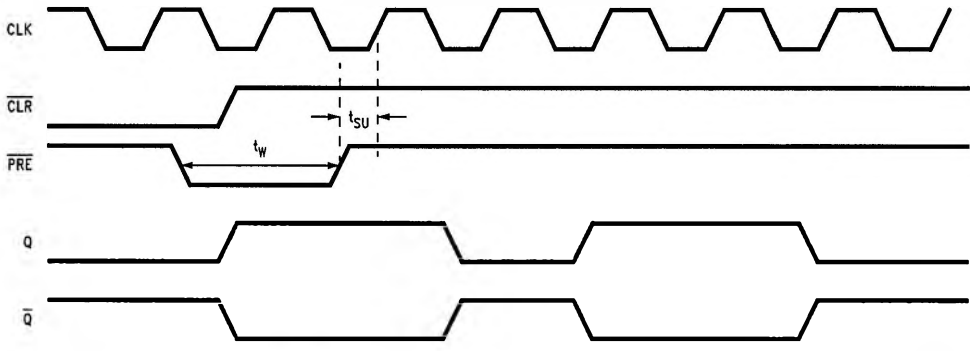
*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the eight outptus. V_{VV} by-pass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers
CGS74B303, CGS74B304, CGS74B305



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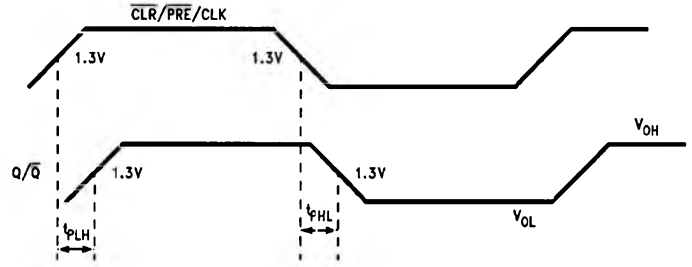

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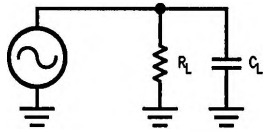
Test Circuit



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R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.
C_L is 30 pF for t_{rise} and t_{fall} measurements.

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.
- Load capacitance includes the test jig.